



The World Leader in High Performance Signal Processing Solutions

## ADI专家面对面：

深入了解16位8通道同步采样数据采集系统AD7606

Customer Application Center, Asia



# Agenda

- ◆ **Introduction to the AD7606 Data Acquisition System**
  - Key features and functions
  - Design hints
  - Typical applications
  
- ◆ **ADI PLM demo**
  
- ◆ **Case studies**
  - Hardware related issues
  - Software related issues



The World Leader in High Performance Signal Processing Solutions

# Introduction to the AD7606 Data Acquisition System



# AD7606 win EDN China 2010 Innovation Award



## EDN China 2010 年创新奖

模拟与  
混合信号

转换类

亚德诺半导体技术(上海)有限公司  
(Analog Devices)

AD7606: 8通道DAS, 内置16位、双极性、同步采样ADC

### 转换类 Converters

产品: AD7606: 8通道DAS, 内置16位、双极性、同步采样ADC

厂商: 亚德诺半导体技术(上海)有限公司(Analog Devices)

评语: AD7606 系列集成最多有八通道的同步采样16位ADC, 可实现90 dB 的 SNR (信噪比), 可选的过采样模式进一步提高了 SNR 性能, 减少了代码扩展, 并增强了抗混叠能力。可提供下一代电力线监控系统设计所需的分辨率和性能, 现有用户可以通过该产品对原有系统进行有效的升级, 从而增强市场竞争力。



# AD7606 16 bit, 8 channel Data Acquisition System

**Released**

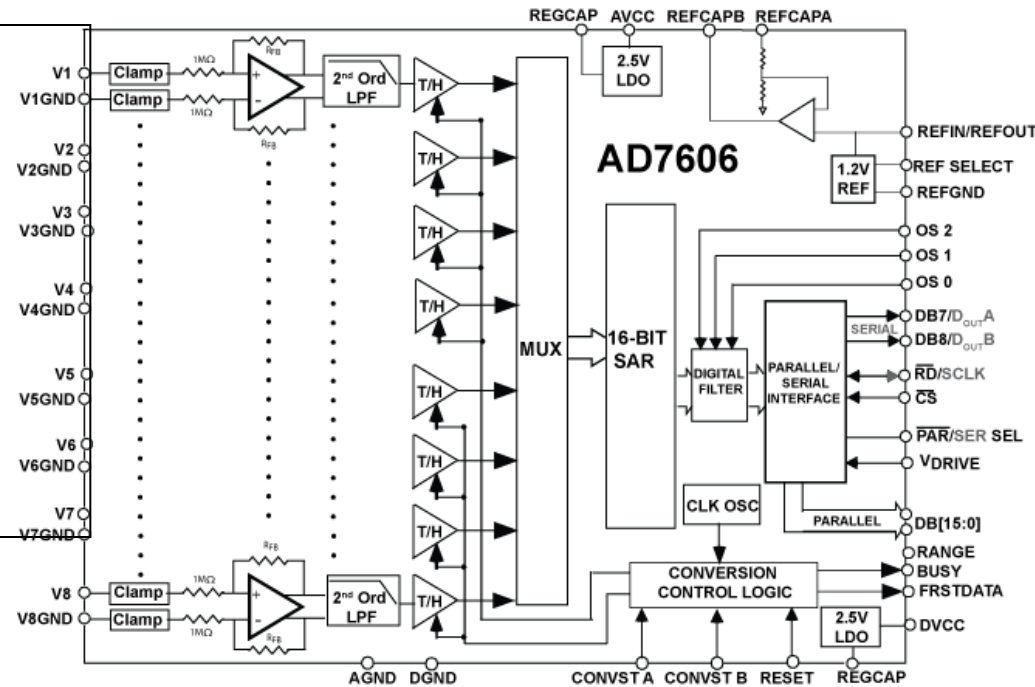
## Features

- ◆ 8 simultaneous sampling channels
- ◆ Single 5V supply operation
- ◆ +-10V +-5V bipolar input
- ◆ Analog input clamp protection
- ◆ 1Meg Resistor input impedance
- ◆ 2<sup>nd</sup> Order Analog Anti-Alias Filter
- ◆ Flexible Digital filter
- ◆ 2.5V reference and reference buffer
- ◆ Serial and Parallel interface.

- ◆ 64 lead LQFP Package

## Performance

- ◆ 90dB SNR @ 200k
- ◆ 96dB SNR @ 12.5k (digital filter)
- ◆ 100mW Power
- ◆ INL +/- 2 LSB, 16 Bit NMC
- ◆ Input Clamps to +-16.5V
- ◆ NFS/PFS Code 8 LSB @ 25
- ◆ NFS/PFS Code 32 LSB max



### AD7606-4/AD7606-6

- ◆ As per AD7606 except
  - 4,6 channel

### AD7607

- ◆ As per AD7606 except
  - 14-Bit

### AD7608/AD7609

- ◆ As per AD7606 except
  - 18-Bit S.E. / 18-Bit Diff
  - preliminary

# AD7606 DAS Benefits



1MΩ Analog Inputs saves on external buffers

Single 5V supply saves on negative supply rail

Fewer Decoupling Caps simplify PCB design, improve performance and reduce BOM

Input Clamp protection to ±16.5V

Analog Anti-alias Filter

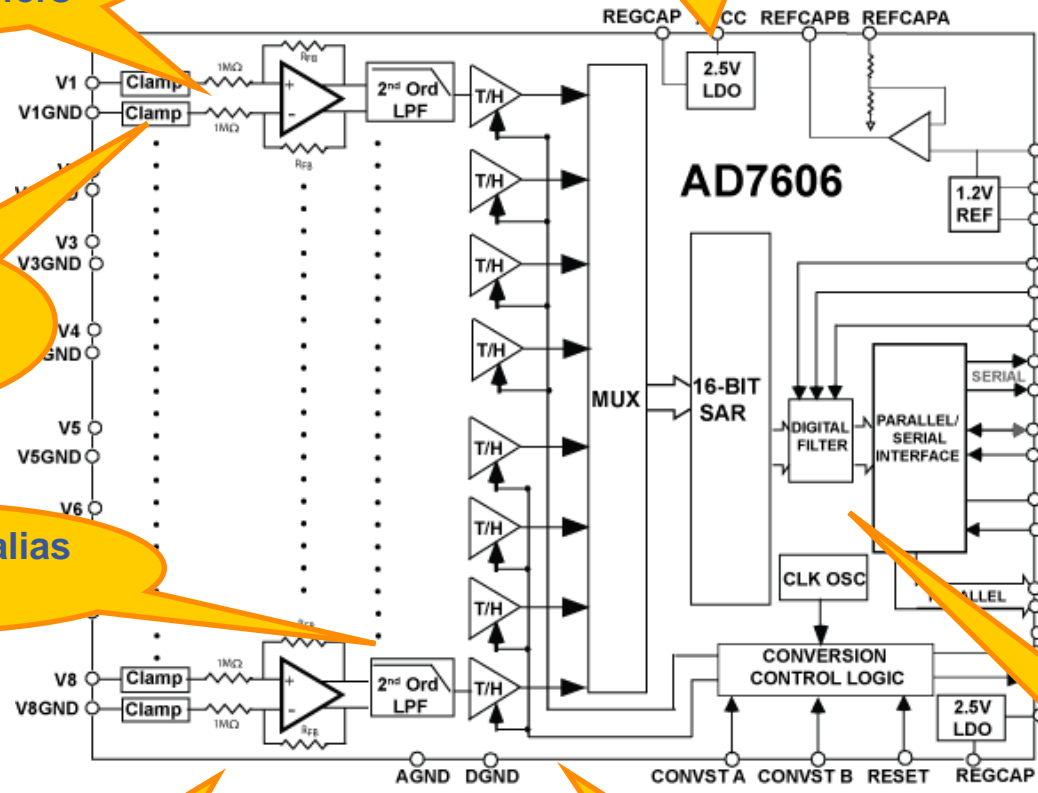
**SNR 96dB!**

**TUE ±12 LSB**

~same power as AD7656 - plus 2 more channels and integration!

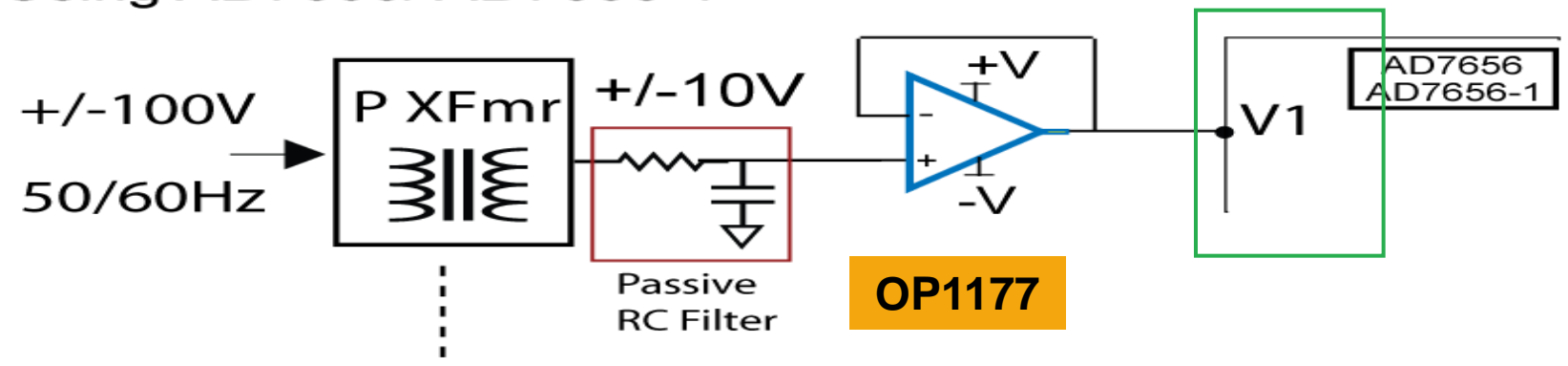
64-ld LQFP Package

Digital Filter



# AD7606 Front End Integration

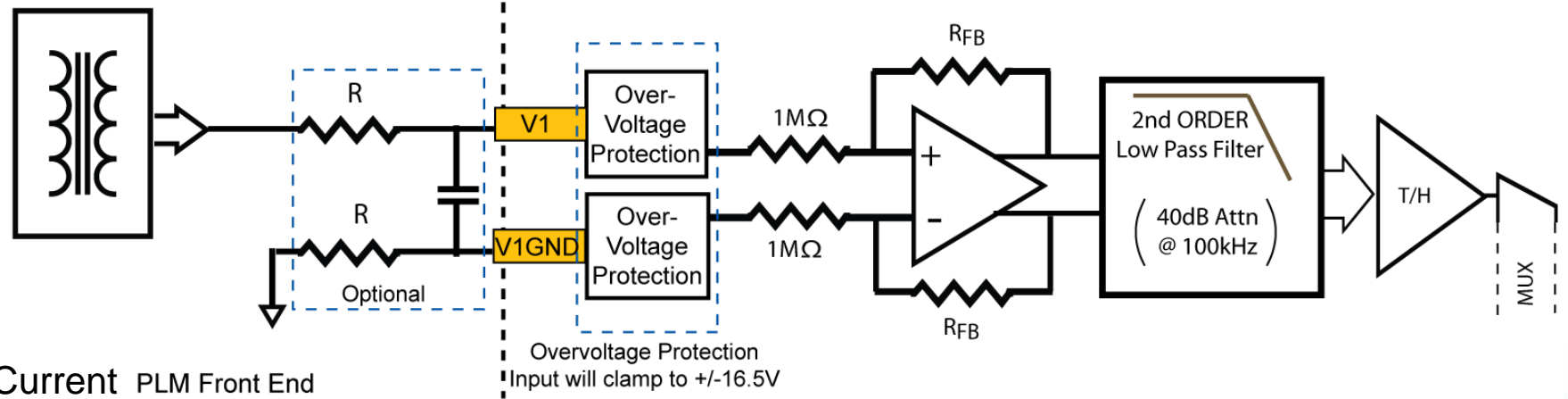
Using AD7656/ AD7656-1



Previous PLM front end

Using AD7606 - 1 Channel Shown

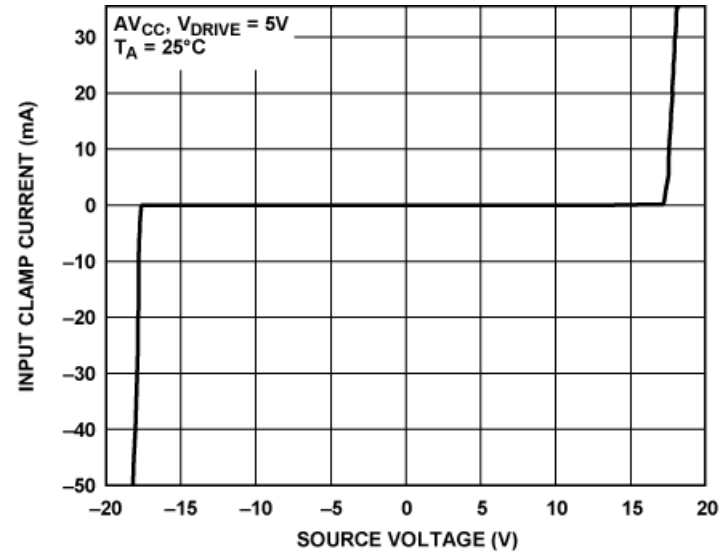
FOCUS: ONE INPUT CHANNEL OF AD7606



Current PLM Front End

# AD7606 Analog input Clamps

- ◆ **AD7606 clamps to  $\pm 16.5V$  in fault condition.**
- ◆ **Input current must be limited to  $\pm 10mA$  for fault voltages  $> \pm 16.5V$ .**
- ◆ **ESD performance on Analog Inputs 7kV HBM**



**AD7606**

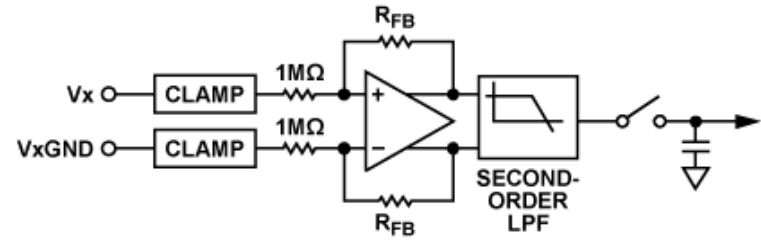
08479-033



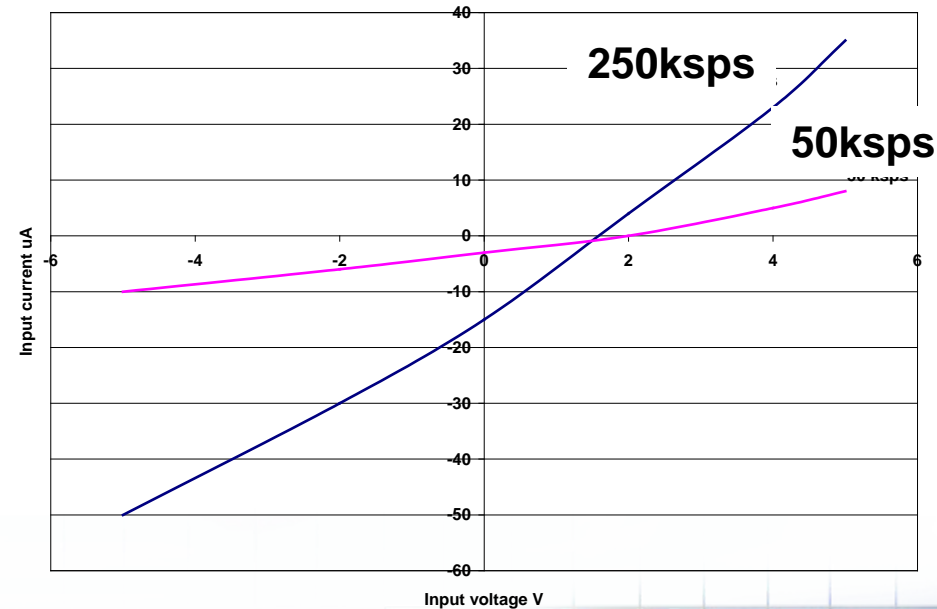
# Analog input impedance

- ◆ AD7606 analog input impedance is fixed at 1 MOhm.
- ◆ The input current ( $\mu\text{A}$ ) required to drive the AD7606 is fixed regardless of  $F_{\text{sample}}$ .
- ◆ Capacitive input - impedance is dependant on the  $F_{\text{sample}}$
- ◆ As  $F_{\text{sample}}$  increases the current required to drive the analog inputs will increase.
- ◆ Example shown where ADC X input current is a function of  $F_{\text{sample}}$ .
- ◆ Regardless of  $F_{\text{sample}}$  the AD7606 does not need an input buffer.

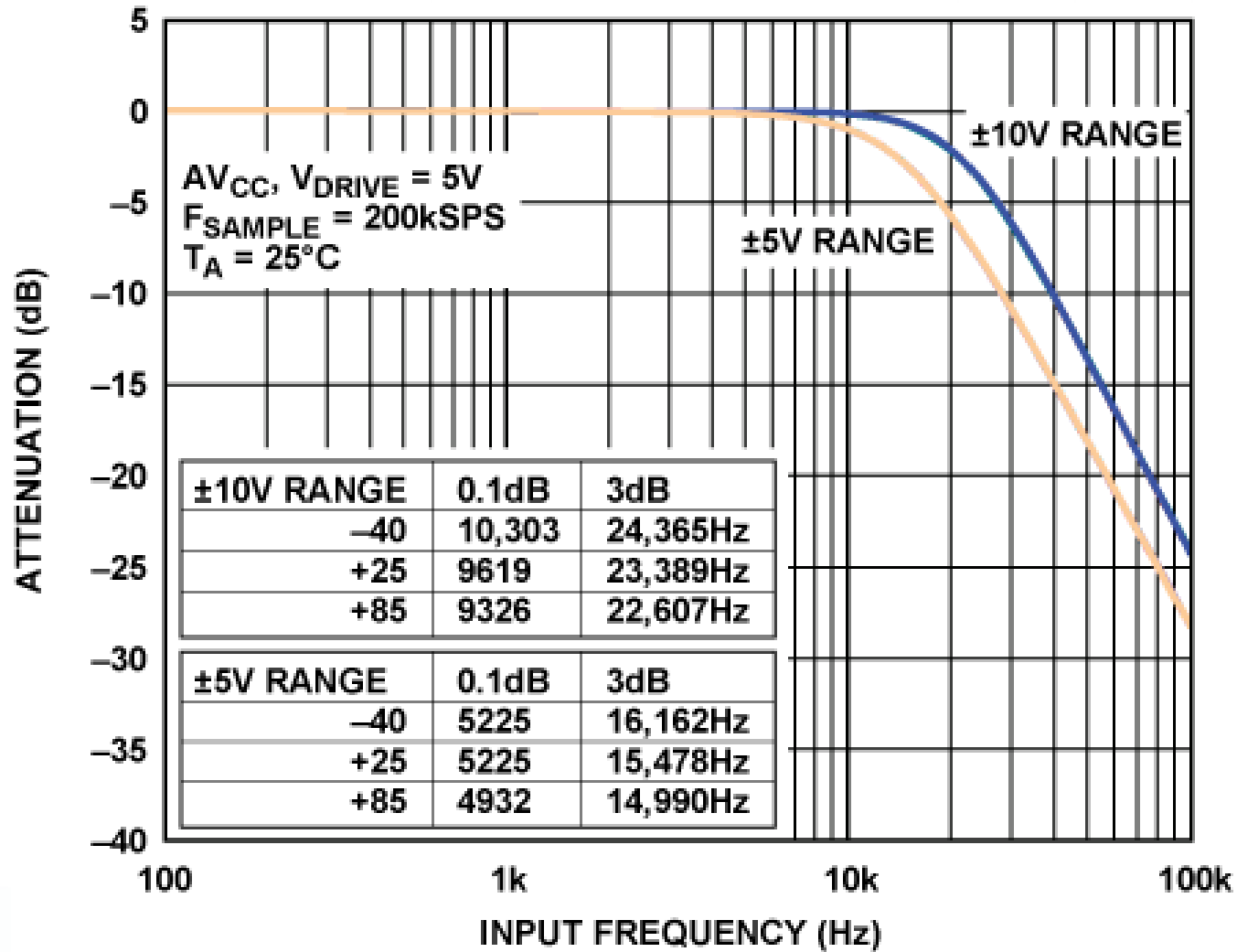
## AD7606



## Input current vs $F_{\text{sample}}$

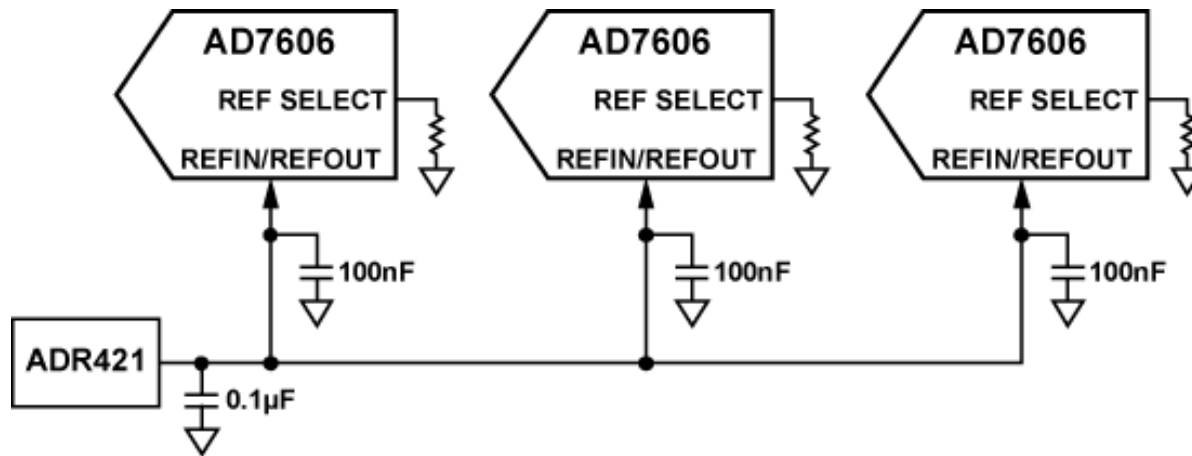


# AD7606 Antialias Filter Frequency Response



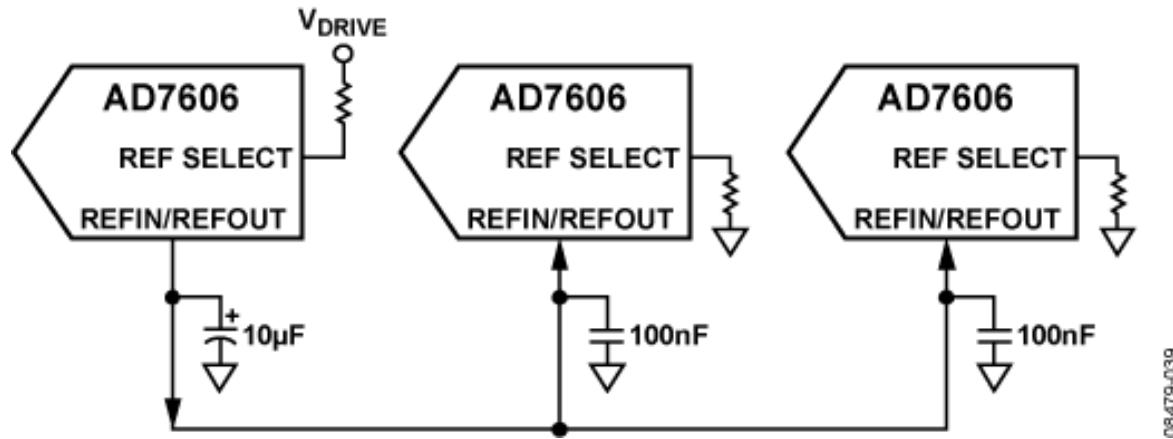
08479-035

# AD7606 Using external reference



- ◆ Where absolute gain PFS error is important an external reference should be used for multiple ADCs
- ◆ Ideal code =  $V_{in}/10V * 2^{15}$
- ◆ Actual code =  $V_{in}/10V * 2^{15} * (REFIN/2.5V)$
- ◆ Choose a tight tolerance reference with low drift when absolute gain error is important.

# AD7606 Using Internal reference



- ◆ Where PFS error matching is important the internal ref on one AD7606 can be used as the ref for other AD7606 devices.
- ◆ If the same reference is used for multiple AD7606 devices **ANY** channel on **ANY** AD7606 device will always be within 32 codes of any other AD7606 channel (irrespective of temperature)

# AD7606 Digital Filter

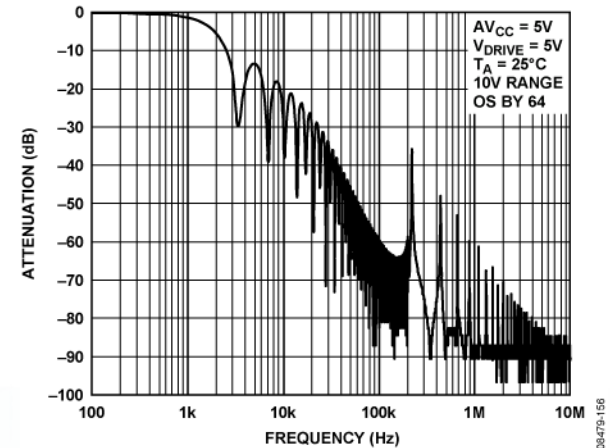
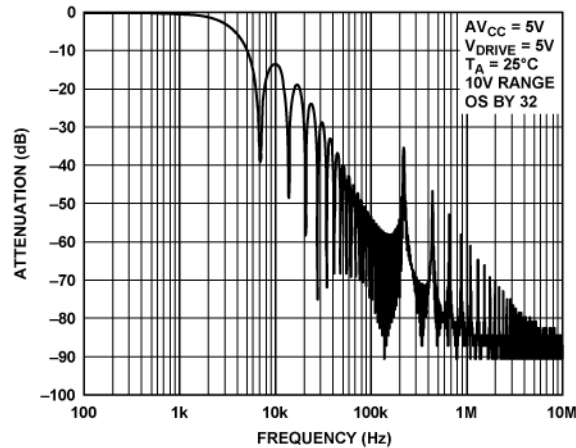
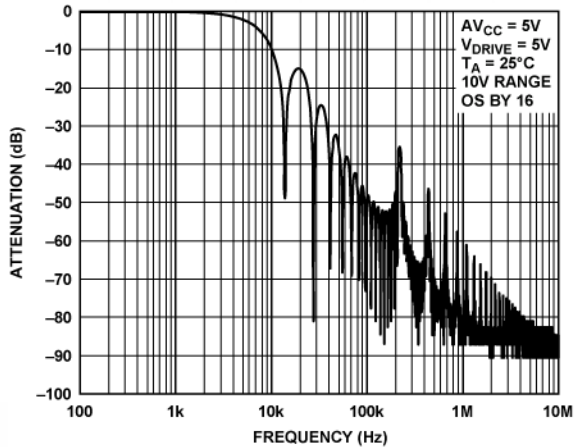
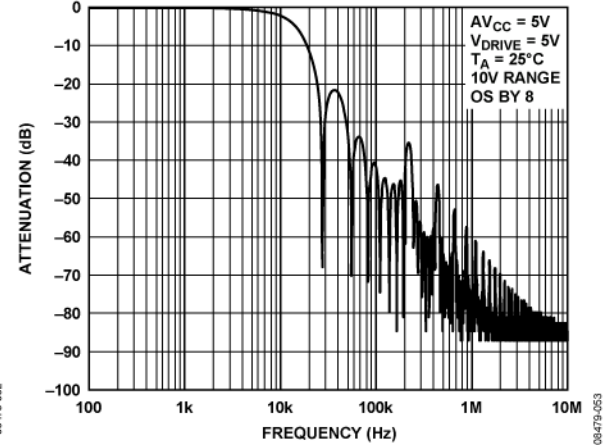
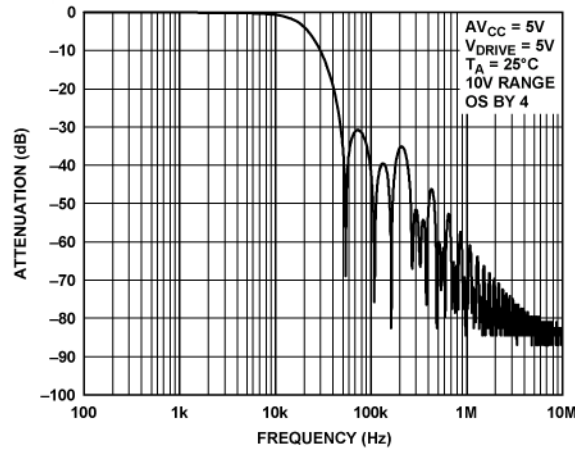
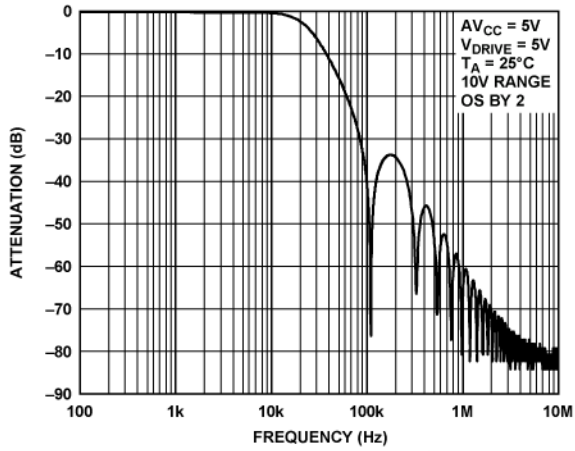
- **Easy to use -> Pin driven**
  - ◆ OS 2, OS 1, OS 0
- **Oversampling ratio**
  - ◆ 2x, 4x, 8x, 16, 32x, 64X
- **Digital Filter is a sinc filter**
  - ◆ simply accumulates, averages and decimates
- **Features of Digital Filter**
  - ◆ Improves SNR by 3dB for every doubling in oversampling ratio
  - ◆ decreases thrupt by 2X by every doubling in oversampling ratio
  - ◆ Reduces analog input 3dB bandwidth by increasing oversampling ratio
- **AD7606 analog anti-alias filter, ADC and digital filter is the complete Data Acquisition System.**

# Digital Filter

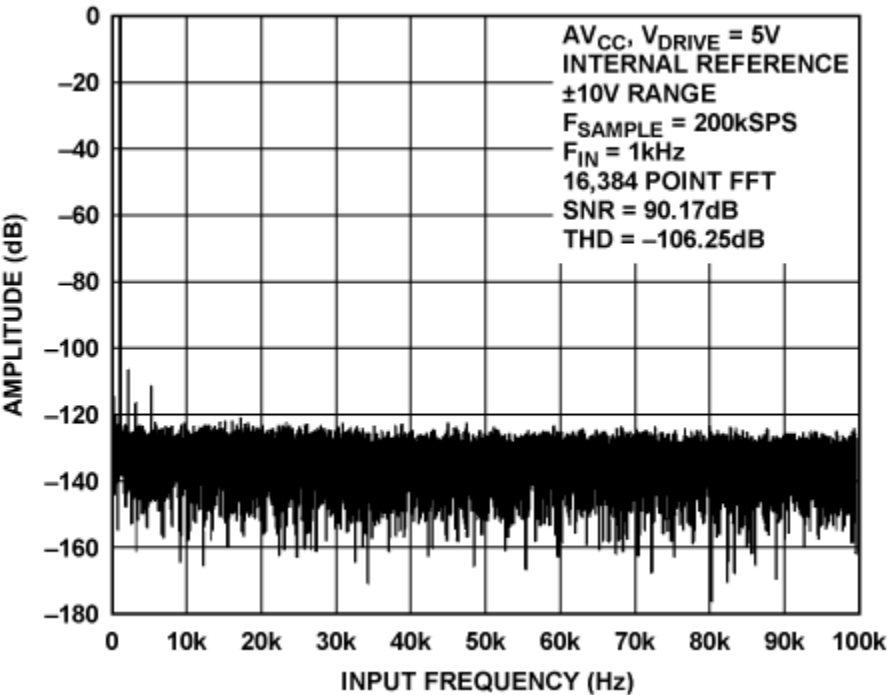
OS[2:0]	OS Ratio	SNR 5 V Range (dB)	SNR 10 V Range (dB)	3 dB BW 5 V Range (kHz)	3 dB BW 10 V Range (kHz)	Maximum Throughput CONVST Frequency (kHz)
000	No OS	89	90	15	22	200
001	2	91.2	92	15	22	100
010	4	92.6	93.6	13.7	18.5	50
011	8	94.2	95	10.3	11.9	25
100	16	95.5	96	6	6	12.5
101	32	96.4	96.7	3	3	6.25
110	64	96.9	97	1.5	1.5	3.125
111	Invalid					

- ◆ **SNR improves as OS rate increased**
- ◆ **3dB Bandwidth reduces**
- ◆ **Maximum allowed CONVST sample rate reduces**

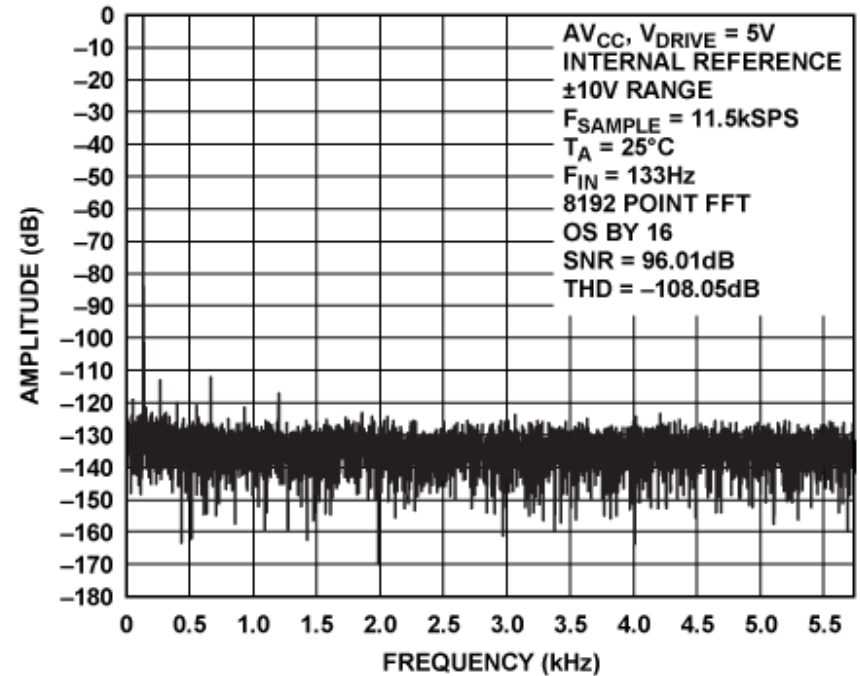
# Digital Filter Responses by OS Rate



# Benefit of Oversampling



No Oversampling



Oversampling x 16



# Histogram of Codes (No OS to OS32)

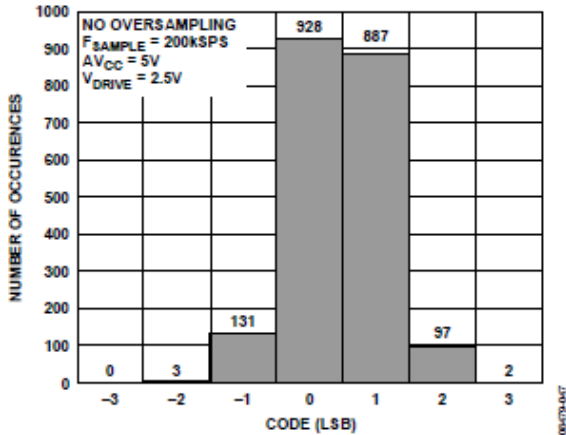


Figure 49. Histogram of Codes—No OS (Six Codes)

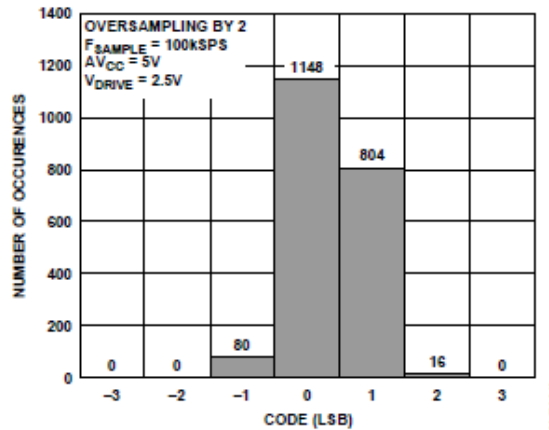


Figure 50. Histogram of Codes—OS  $\times$  2 (Four Codes)

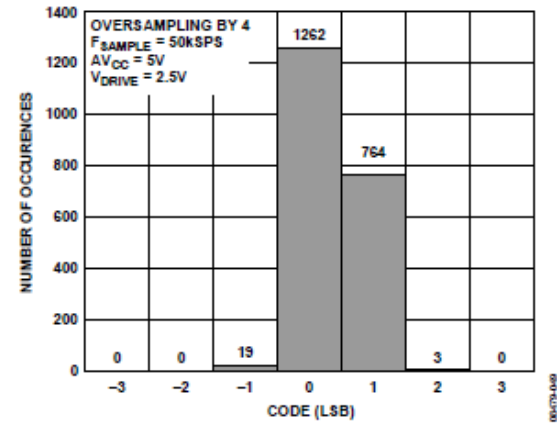


Figure 51. Histogram of Codes—OS  $\times$  4 (Four Codes)

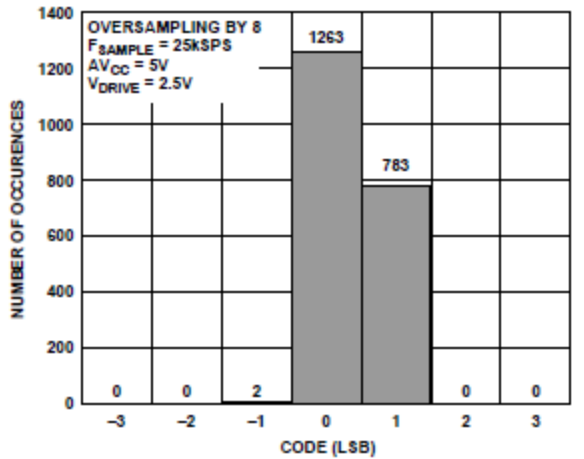


Figure 52. Histogram of Codes—OS  $\times$  8 (Three Codes)

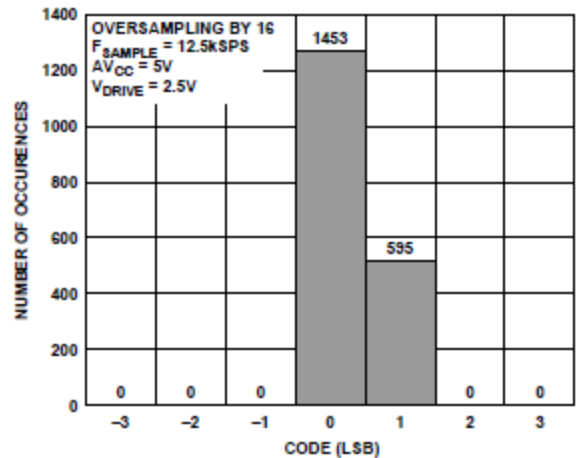


Figure 53. Histogram of Codes—OS  $\times$  16 (Two Codes)

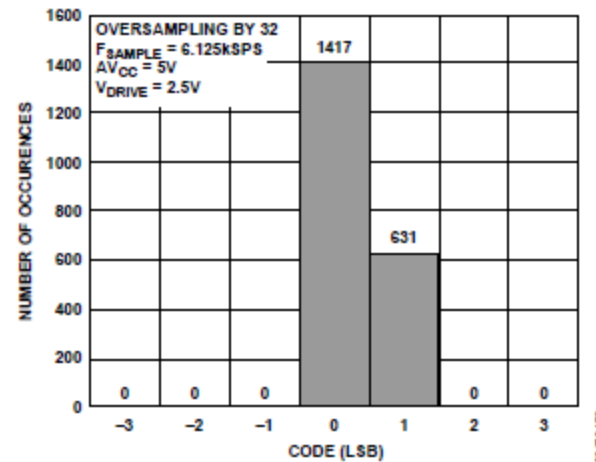
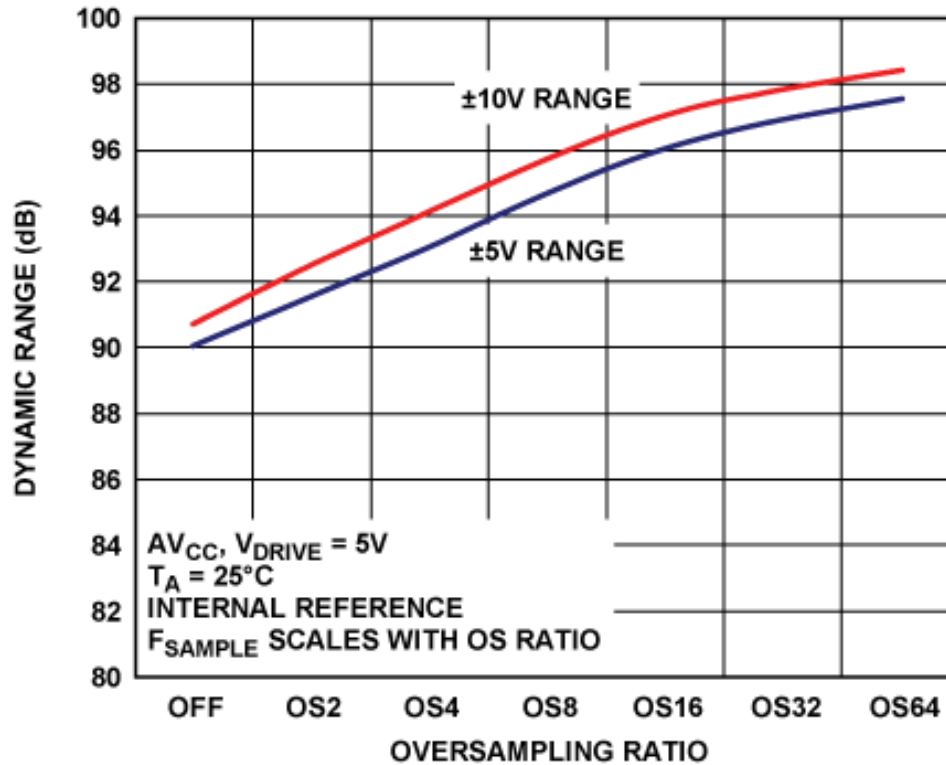


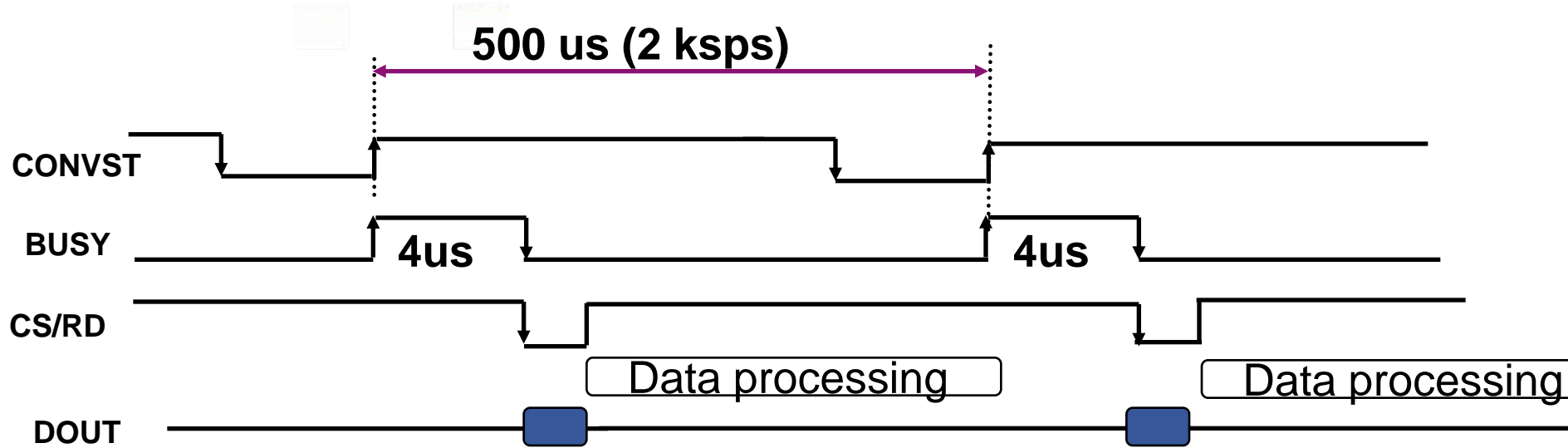
Figure 54. Histogram of Codes—OS  $\times$  32 (Two Codes)

# Oversampling Increases Dynamic Range



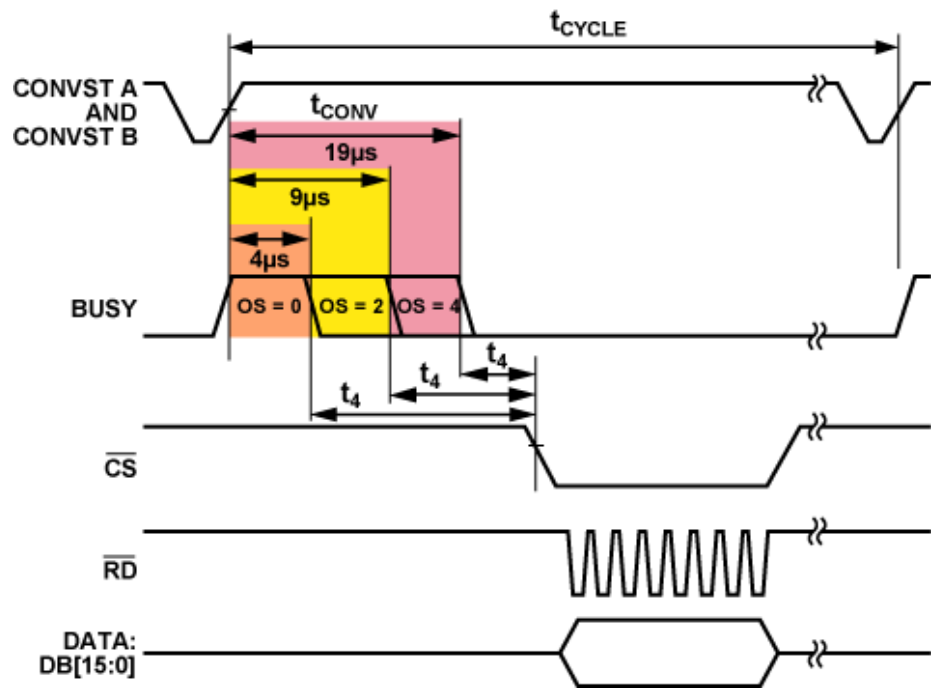
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# Current Interface Solution (AD7606-OS off)



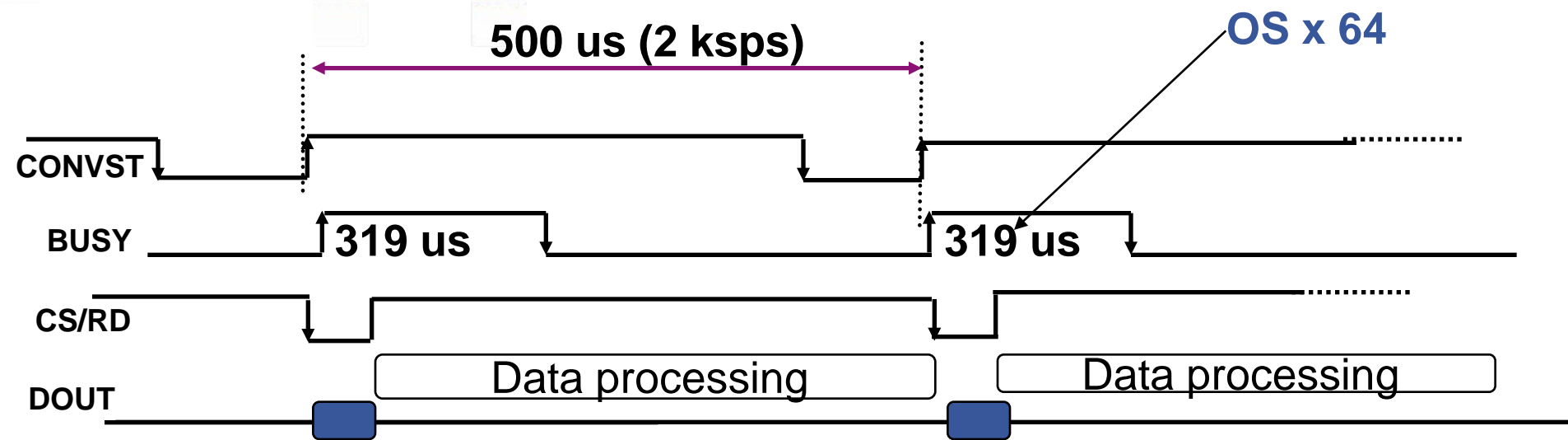
- ◆ All channels are read after the BUSY high time.
- ◆ Depending on the number of ADC devices on the boards, could be up to ~ 495 us processing time.
- ◆ But with the AD7606, a read is allowed during conversion and CONVST can idle high or low

# Oversampling extends BUSY High Time



08479-046

# AD7606 over sampling solution



- ◆ **CONVST rising edge** could be used to trigger a read from the AD7606 during conversion.
- ◆ A read of all 8 AD7606 channels is ~ 240 ns.
- ◆ CONVST rising edge will start a new conversion.
- ◆ This method of using the AD7606 will have little effect on data processing time.
- ◆ It will yield benefits in noise performance and code spread.

# Substation Automation Design Examples

## ◆ Purpose of examples

- Compare AD7606 versus traditional bipolar input ADC (ADC X)
- How to best use AD7606 analog and digital filters.

## ◆ AD7606

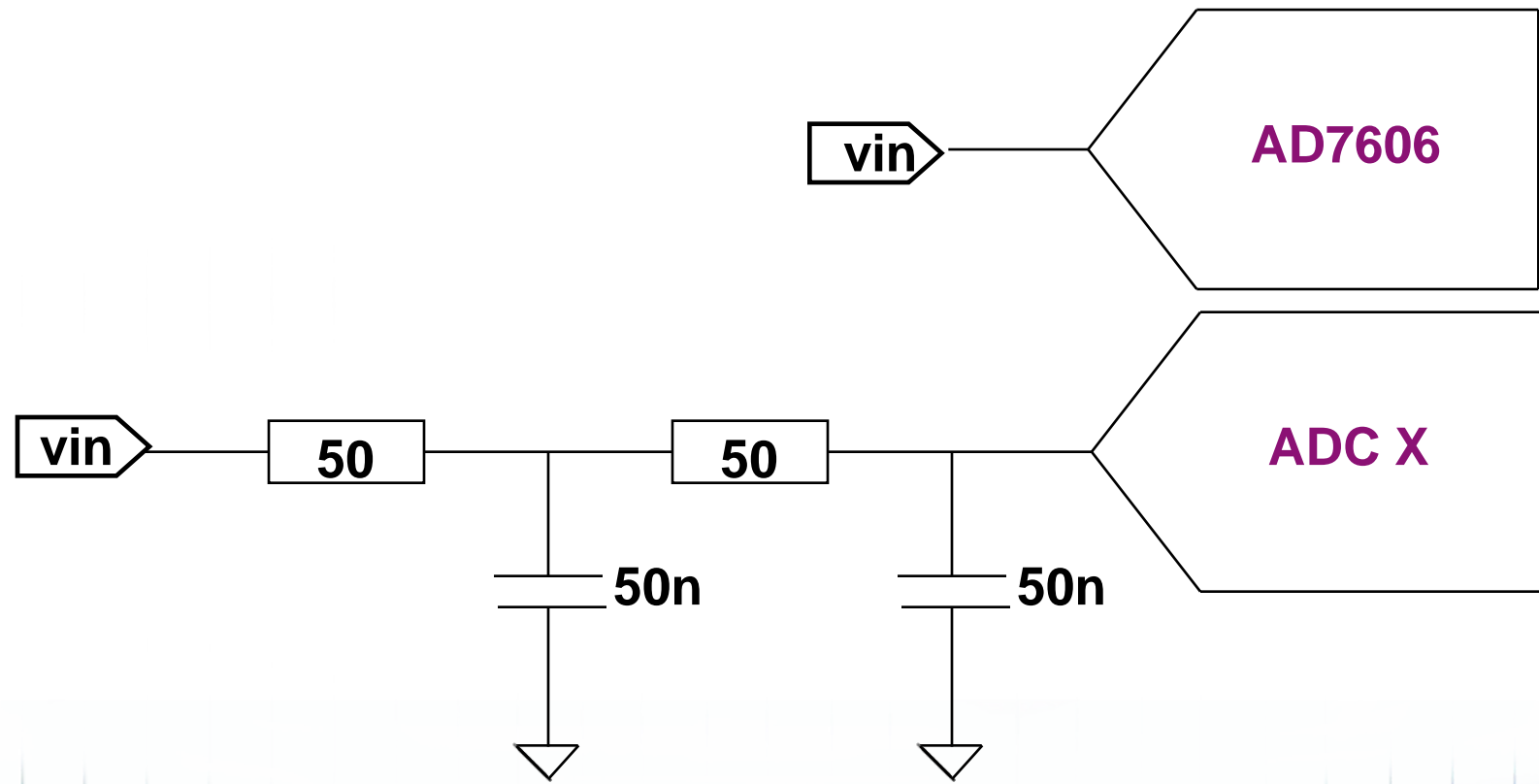
- 1Meg resistor input, impedance fixed with thruput.
- Integrated 2<sup>nd</sup> order anti-alias active low pass filter
- Integrated digital sinc low pass filter

## ◆ ADC X (other bipolar ADCs e.g. AD7656)

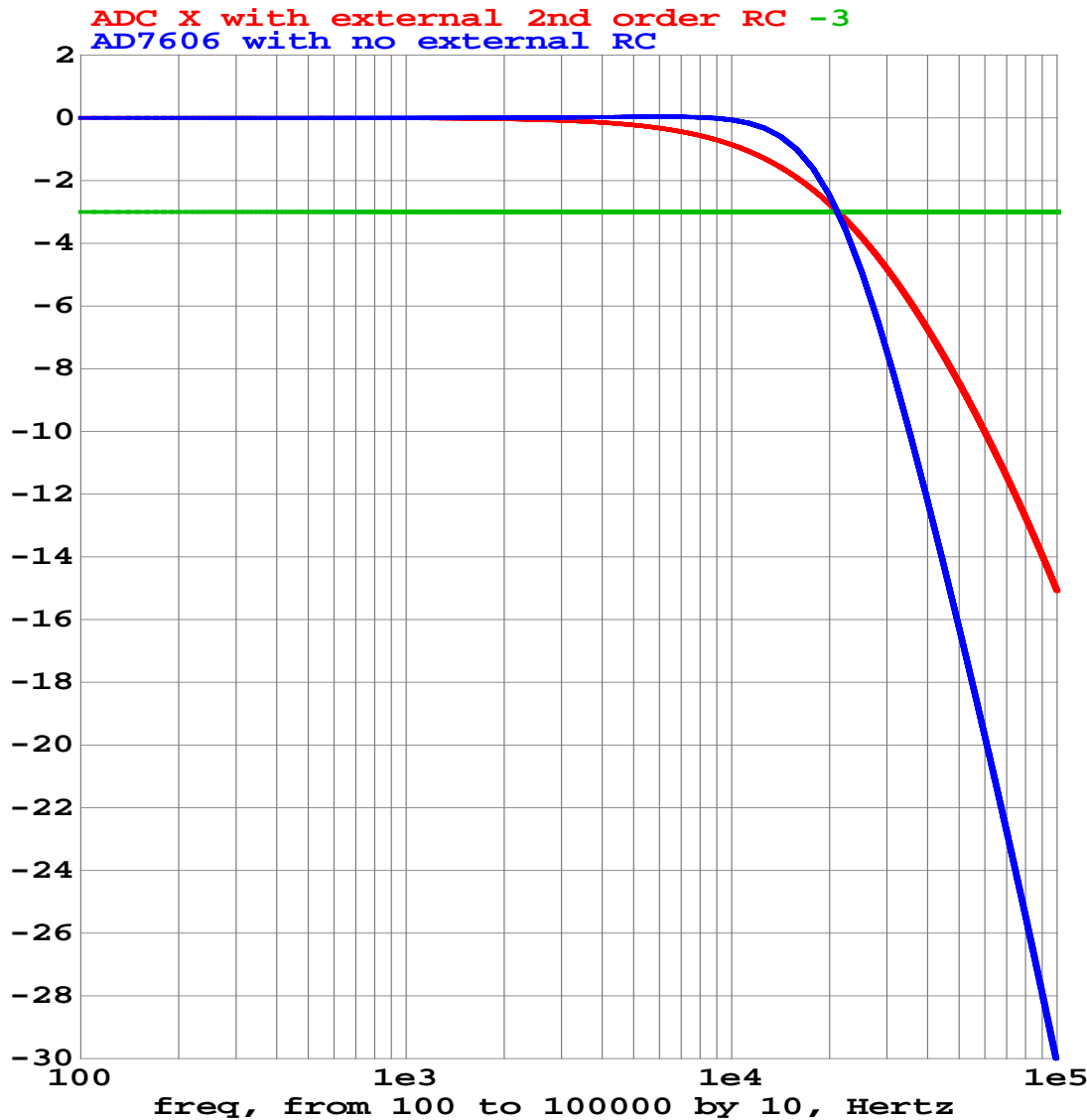
- Capacitor input, impedance varies with throughput
- No on chip analog anti-alias filter
- No on chip Digital Filter

# Example 1: Need a 22kHz -3dB bandwidth

- AD7606 -> using internal 2<sup>nd</sup> order active analog filter, digital filter disabled (no external circuitry required)
- ADC X -> with external 2<sup>nd</sup> order RC



# Example 1: Need a 22kHz -3dB bandwidth



**ADC X with 2<sup>nd</sup> order RC**  
3db Freq = 22kHz  
0.1db freq = 3.4kHz  
Attenuation @100kHz = -15dB

**AD7606 with internal filters**  
3db Freq = 22kHz  
0.1db freq = 10kHz  
Attenuation @100kHz = -30dB

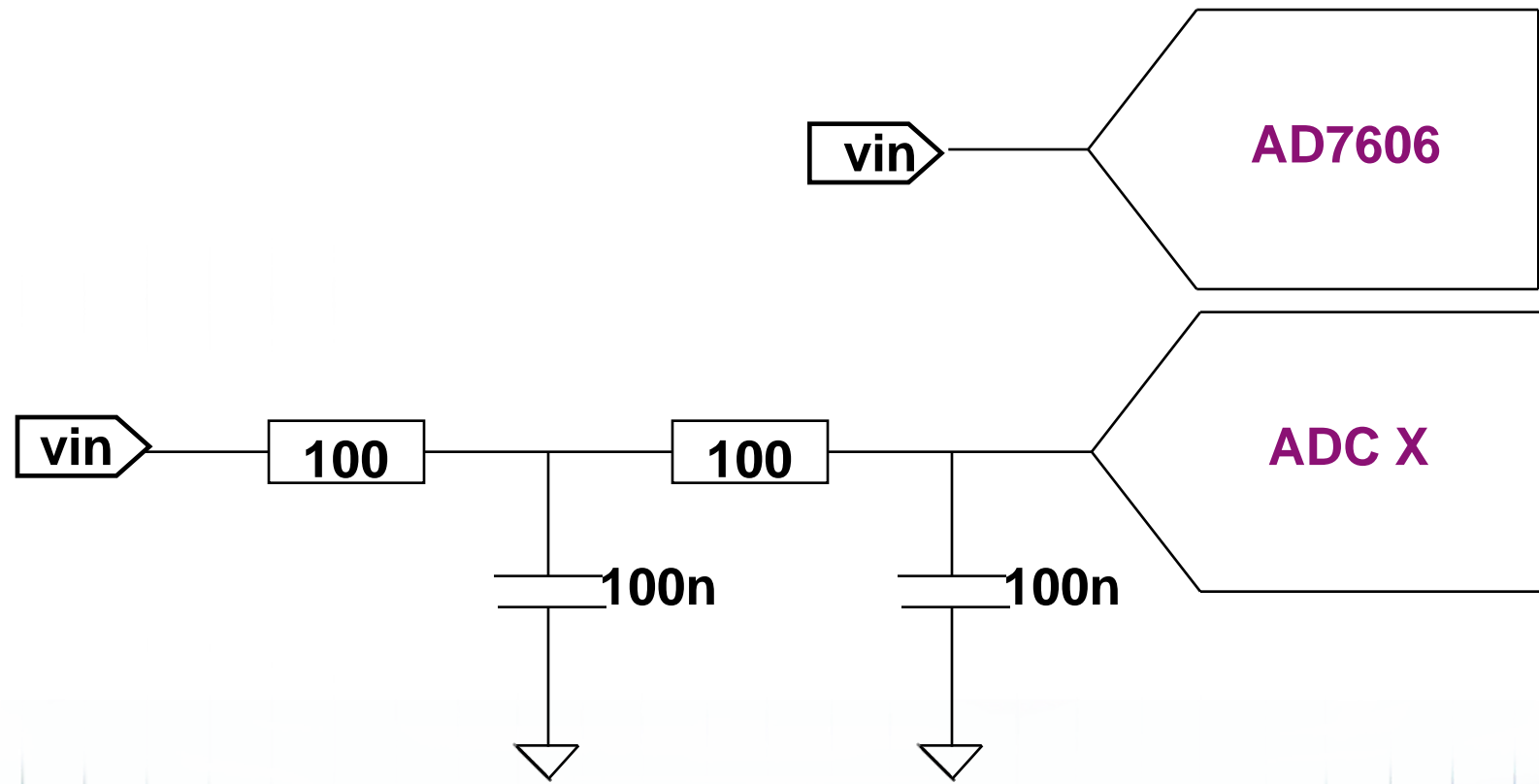
**External R-C filter has  
attenuation in pass band.**

**AD7606 internal filter is 2<sup>nd</sup>  
order active which is optimised  
for gain flatness in pass band  
and good roll off at higher  
frequencies.**

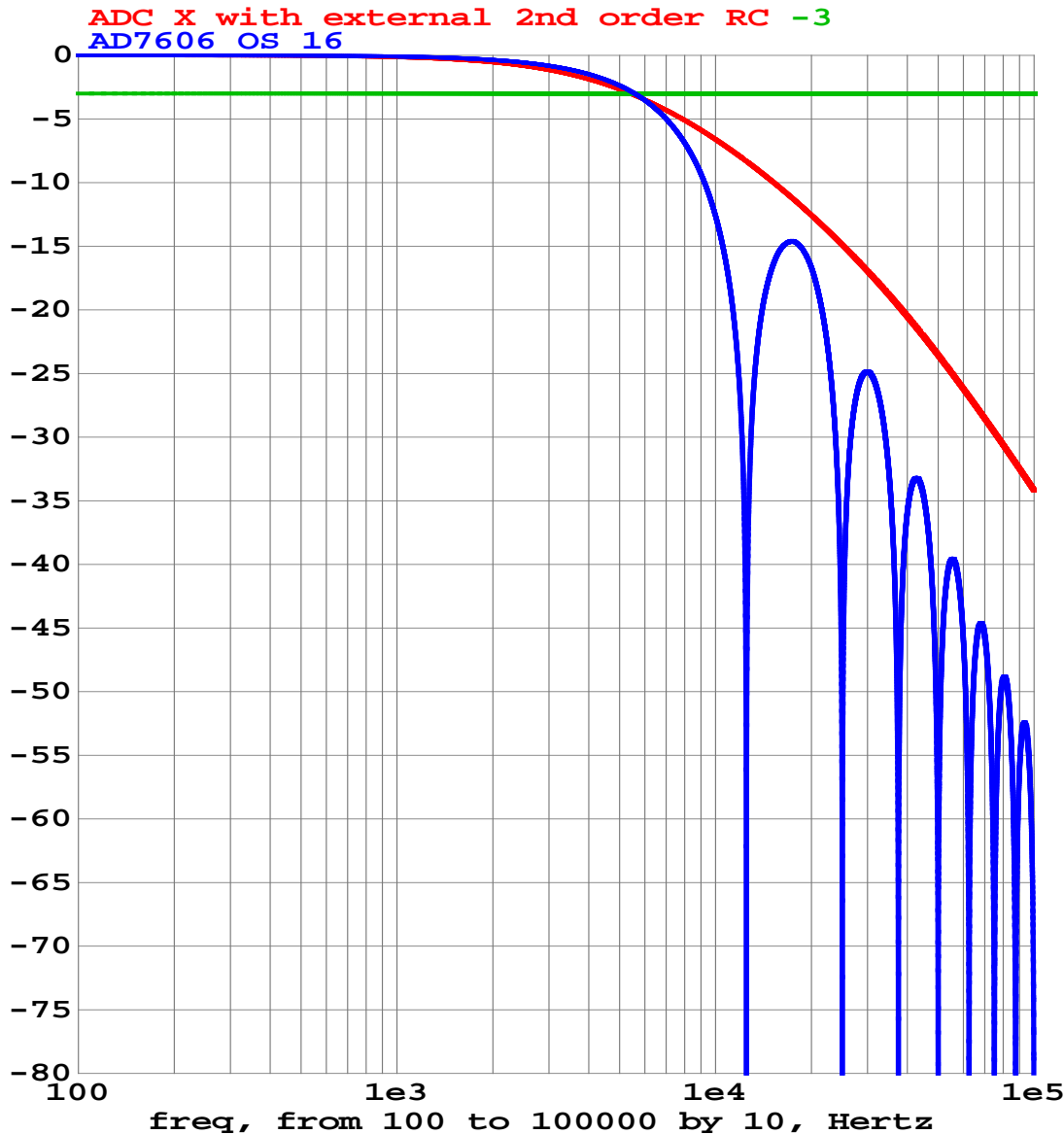


# Example 2: Need a 5.5kHz -3dB bandwidth

- AD7606 -> using internal 2<sup>nd</sup> order active analog filter and internal digital filter enabled (OS 16)
- ADC X -> with external 2<sup>nd</sup> order RC



# Example 2: Need a 5.5kHz -3dB bandwidth



**ADC X with 2<sup>nd</sup> order RC**  
3db Freq = ~5.5kHz  
0.1db freq = 830hZ  
Attenuation @100kHz = -35dB

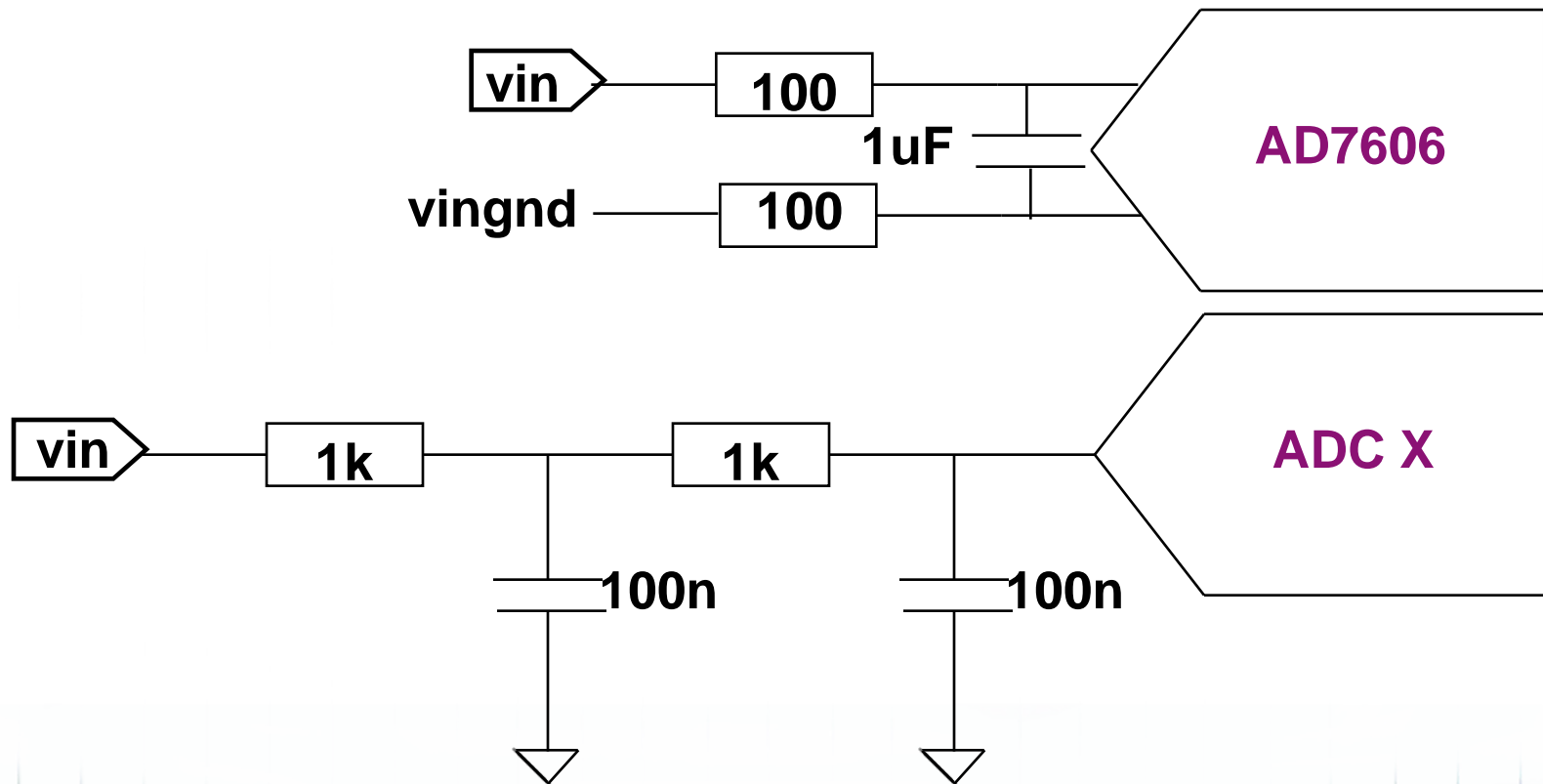
**AD7606 with internal filters**  
3db Freq = ~5.5kHz  
0.1db freq = 1100hZ  
Attenuation @100kHz = -55dB

**AD7606 digital filter reduces 3dB frequency and improves SNR.**

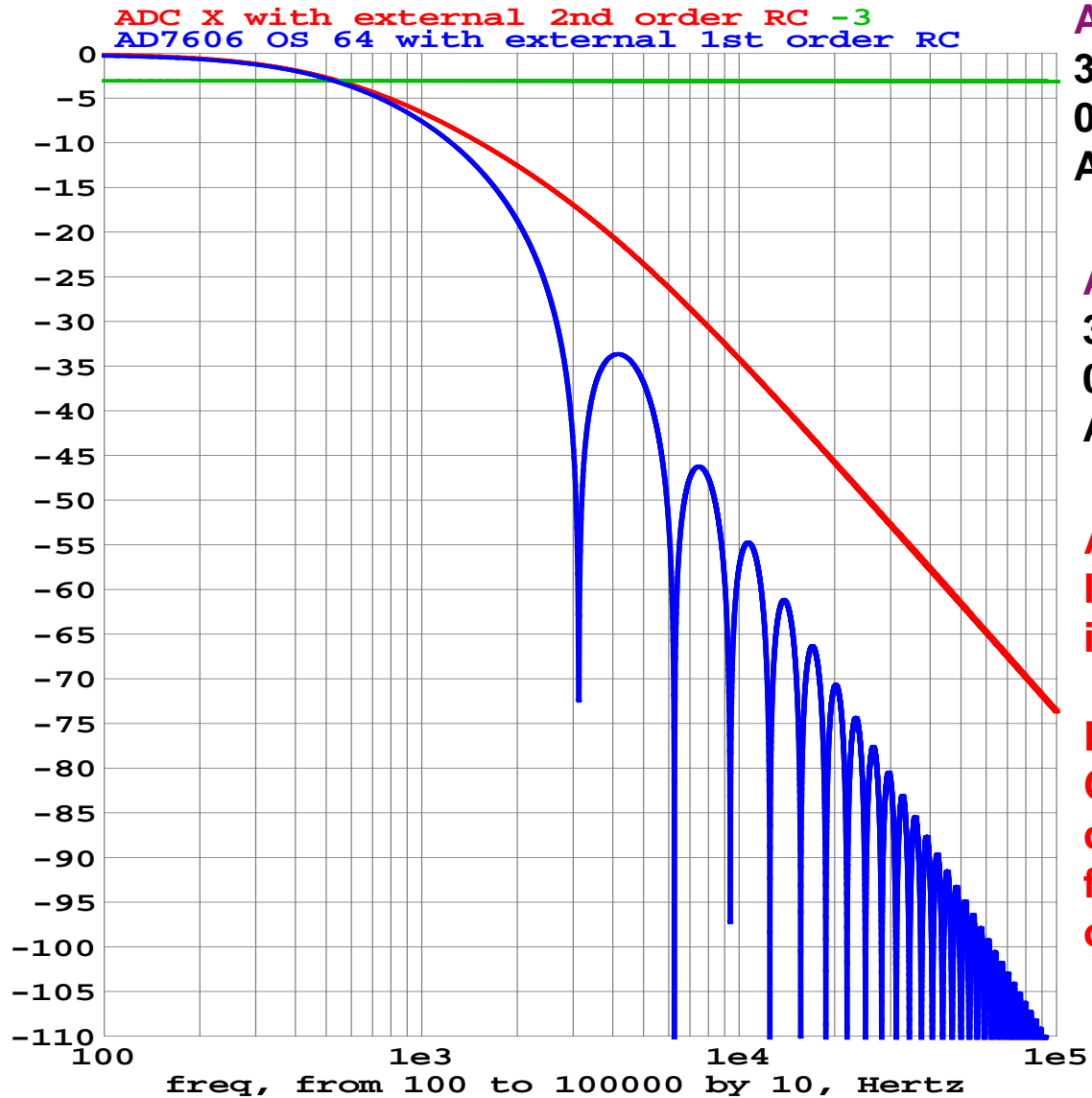
**For more rejection align CONVST sample frequency on divisions of internal sampling frequency (200ksps). This example optimum is 12.5kHz (200k/16)**

## Example 3: Need a 550Hz -3dB bandwidth

- AD7606 -> using internal 2<sup>nd</sup> order active analog filter, internal digital filter enabled (OS 64) and external 1<sup>st</sup> order RC
- ADC X -> with external 2<sup>nd</sup> order RC



# Example 3: Need a 550hZ -3db bandwidth



**ADC X with 2<sup>nd</sup> order RC**

**3db Freq = 550hZ**

**0.1db freq = 80hZ**

**Attenuation @100kHz = -75dB**

**AD7606 with internal filters**

**3db Freq = 550hZ**

**0.1db freq = 80hZ**

**Attenuation @100kHz = -110dB**

**AD7606 digital filter reduces  
lowers 3dB frequency and  
improves SNR.**

**For more rejection align  
CONVST sample frequency on  
divisions of internal sampling  
frequency (200k). This example  
optimum is 3.125kHz (200k/64)**

# ADC X needs an opamp per analog input

- **AD7606 gives a better filter response**
  - ◆ More gain flatness in pass band for wide bandwidth applications
  - ◆ More anti-alias rejection at higher frequencies
- **How to improve filter response of ADC X**
  - ◆ Increase external filter to 3<sup>rd</sup> order.
    - More attenuation in pass band using 3<sup>rd</sup> order RC.
    - Need to be careful with ADC X, external R impacts acquisition time, charging input cap. Can also affect distortion.
    - Need to switch to active filter -> Which means using an op-amp
- **Sample at higher frequency**
  - ◆ ADC X analog impedance varies with throughput.
  - ◆ Sampling at 100ksps requires an op-amp on the analog input as impedance is lower
- **Op-amp**
  - ◆ Need dual supplies on the board for the op-amp.
  - ◆ Op-amp adds noise, power, offset and gain errors and drift to the system.
  - ◆ Increased BOM Cost (8 op-amps) and design challenge to obtain best performance

# AD7606 vs Competition

- ◆ **1 Mohm input impedance and Integrated input amplifier**
- ◆ **Fixed analog input impedance regardless of Fsample.**
- ◆ **±16.5V input over voltage protection**
- ◆ **Integrated AA Filter and Digital Filter**
  - AD7606 AA and Digital filter eliminates the need for complex external filtering circuitry
- ◆ **Wide Dynamic range with Digital Filter**
  - **Up to 98 dB dynamic range**
- ◆ **Superior INL, THD and power specifications**
- ◆ **AD7606 is 33% smaller board solution and 83% cheaper decoupling solution compared to competitor 8 channel solution.**
- ◆ **Pin compatibility from 14 to 18 bits.**

# Family of DAS Solutions

Resolution	Single-Ended Inputs	True Differential Inputs	Number of Simultaneous Sampling Channels
18 Bits	<a href="#">AD7608</a>	AD7609	8
16 Bits	<a href="#">AD7606</a>		8
	<a href="#">AD7606-6</a>		6
	<a href="#">AD7606-4</a>		4
14 Bits	<a href="#">AD7607</a>		8

# Test AD7606 with Evaluation Board



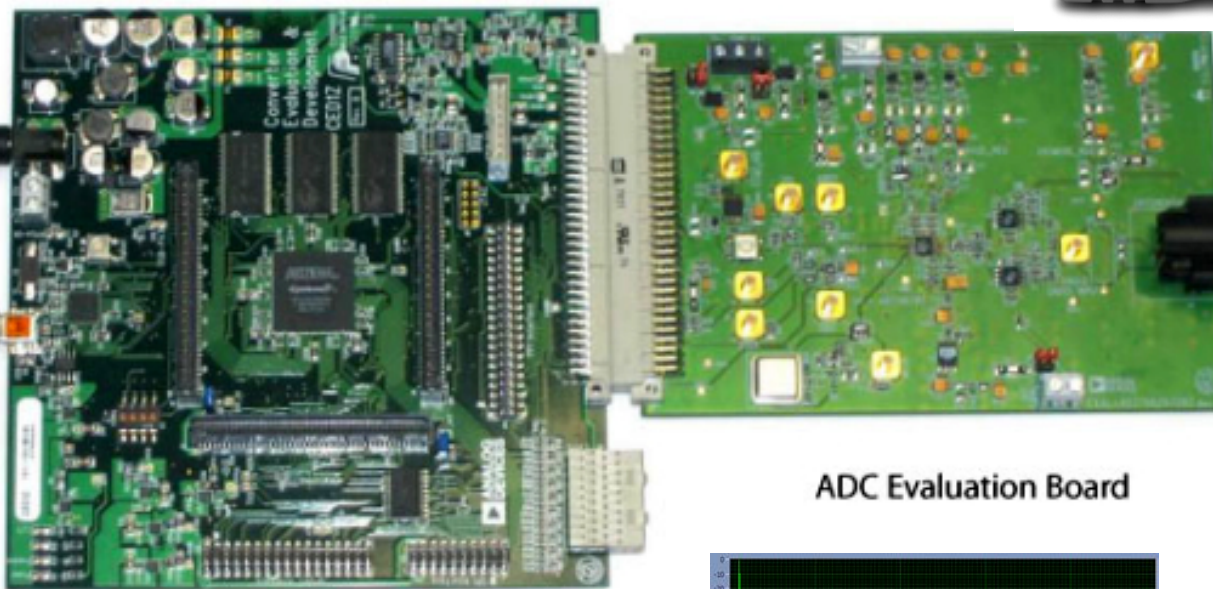
Converter Evaluation & Development Board

Function Generator



Power Supply:  
+7.5v DC @ 2A  
(Provided)

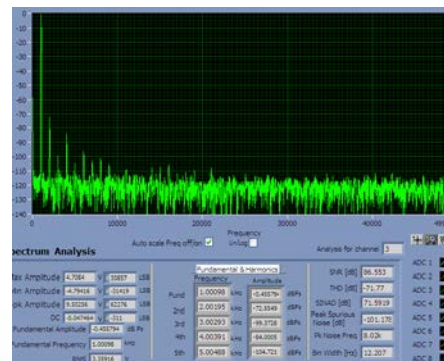
High-speed USB 2.0  
cable (provided)



ADC Evaluation Board



PC Running Windows  
2000 or XP with 1 free  
USB port





# Layout Guidelines

## CN0148 - Layout Considerations for an Expandable Multichannel Simultaneous Sampling Data Acquisition System (DAS) Based on the AD7606 16-Bit, 8-Channel DAS



### Circuit Note CN-0148

**Circuits  
from the Lab**

**Circuit Designs Using Analog Devices Products**  
Apply these product pairings quickly and with confidence.  
For more information and/or support call 1-800-AnalogD  
(1-800-262-5643) or visit [www.analog.com/circuit](http://www.analog.com/circuit).

#### Devices Connected/Referenced

AD7606	8-Channel DAS with 16-Bit, Bipolar, Simultaneous Sampling ADC
AD7606-6	6-Channel DAS with 16-Bit, Bipolar, Simultaneous Sampling ADC
AD7606-4	4-Channel DAS with 16-Bit, Bipolar, Simultaneous Sampling ADC
ADR421	Precision, Low Noise XFET® Voltage Reference

### Layout Considerations for an Expandable Multichannel Simultaneous Sampling Data Acquisition System (DAS) Based on the AD7606 16-Bit, 8-Channel DAS

#### CIRCUIT FUNCTION AND BENEFITS

In power line measurement and protection systems, there is a requirement to simultaneously sample large numbers of current and voltage channels of multiphase power distribution and transmission networks. In these applications, the channel count can vary from as few as six channels to greater than 64 channels. The AD7606 8-channel data acquisition system (DAS) with 16-bit bipolar simultaneously sampling SAR ADCs with on-chip overvoltage protection greatly simplifies signal conditioning circuitry and reduces the overall parts count, board real estate, and cost of the measurement and protection board. Even with its high level of integration, each AD7606 requires only nine low value ceramic decoupling capacitors.

In measurement and protection systems, simultaneous sampling capability is needed to maintain the phase information between the current and voltage channels on multiphase power line networks. The wide dynamic range capability of the AD7606 makes it ideal for capturing both under voltage/current and over voltage/current conditions. The input voltage range is pin-programmable for either  $\pm 5$  V or  $\pm 10$  V.

This circuit note describes details of the recommended PC board layout for applications using multiple AD7606 devices. The layout is optimized for channel-to-channel matching and part-to-part matching and will help reduce the complexity of calibration routines in high channel count systems. The circuit provides the ability to use the AD7606 2.5 V internal reference

two devices yields a level of integration, channel density, and accuracy that is unsurpassed in the industry.

#### CIRCUIT DESCRIPTION

The AD7606 is an integrated, 8-channel data acquisition system with input amplifiers; overvoltage protection; second-order analog antialiasing filters; analog multiplexer; 16-bit, 200 kSPS SAR ADC; and a digital filter—all included on-chip. The circuit shown in Figure 1 consists of two AD7606 devices configurable with the ability to use either the internal 2.5 V reference or an external 2.5 V ADR421 reference. When the REF SELECT pin is connected to a logic high, the internal reference is selected. When the REF SELECT pin is connected to a logic low, the external reference is selected.

The power supply requirements are as follows:  $AV_{CC} = 5$  V,  $V_{DRIVE} = 2.3$  V to 5 V (depending on external logic interface requirements).

This circuit note describes the layout and performance of an evaluation board that contains two AD7606's, making a 16-channel data acquisition system. Complete 16-channel DAS PC board documentation is available at [www.analog.com/CN0148\\_PCB\\_Documentation](http://www.analog.com/CN0148_PCB_Documentation).

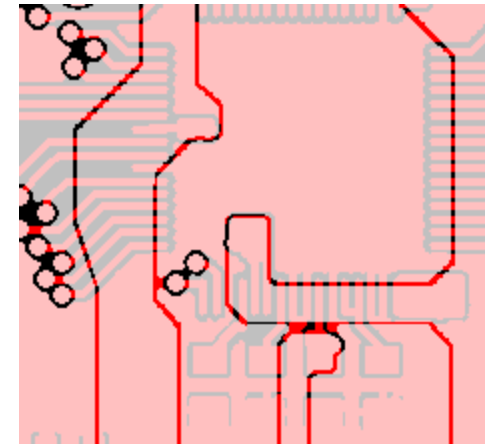
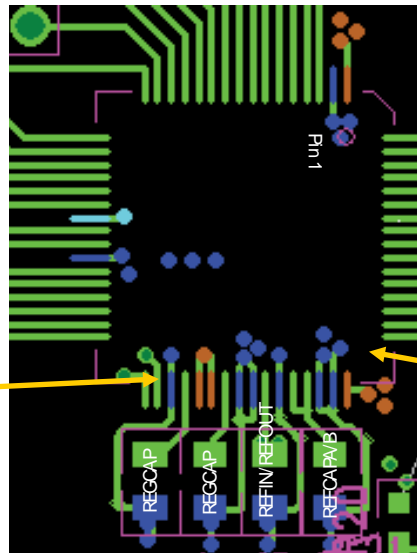
Symmetrical layout around the analog input channels and device decoupling is important for good channel-to-channel matching and part-to-part matching. Data is shown to support the matching performance obtainable with the 16-channel ADC

# Decoupling for the AD7606

- ◆ REFIN/REFOUT, REFCAPA, REFCAPB and REGCAP pins are critical caps for the AD7606 performance.
- ◆ Ideally these caps should be placed on the same side of the board as the AD7606 device.

## Parallel Bus

Low impedance path to GND - Pins grounded to the north and south of pin

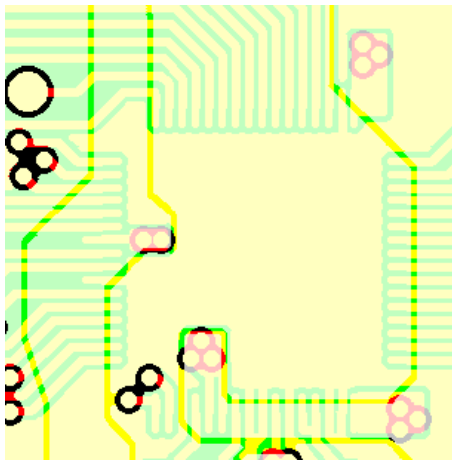


## Analog Inputs

Multiple vias to connect to GND plane

# Bottom layer decoupling for the AD7606

- ◆ Use the bottom layer for power supply decoupling caps.
- ◆ AVCC and VDRIVE decoupling located on bottom layer.



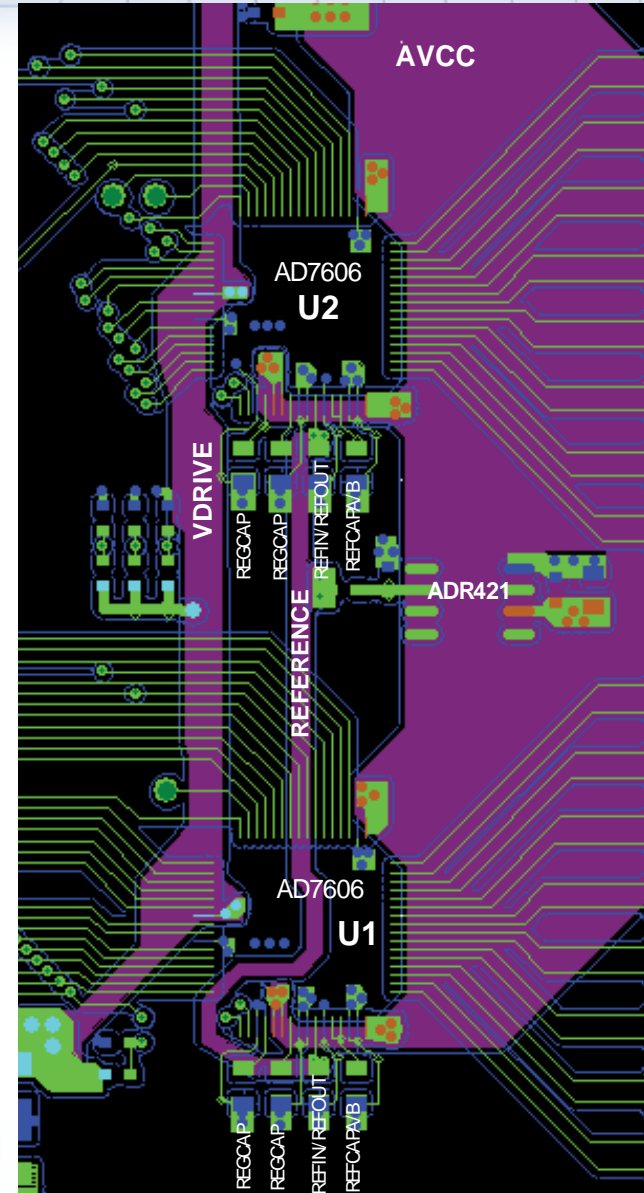
Can share  
decoupling  
cap if placed  
close to pins  
(37,38)



Multiple vias  
used to  
connect to  
the supply  
track/plane

# Power Supply routing

- ◆ Use large traces for the supply tracks.
- ◆ Ideally use a power plane.
- ◆ Layer 3 is dedicated to supply and reference routing and also ground.
- ◆ AVCC supply runs to the right of the device.
- ◆ VDRIVE track runs to the left of the device.
- ◆ Reference ADR421 is located between U1 and U2.
- ◆ The reference voltage track runs north to U1 and south to U2



# Grounding for the AD7606

- ◆ Use large area ground planes for low impedance return paths.
- ◆ Dedicate at least 40 % of connector pins for ground.
- ◆ In a 4 layer board, at least one layer should be dedicated for the ground plane.
- ◆ In a greater than 4 layer board multiple layers should be dedicated for ground planes and these should be evenly distributed throughout the layer stack.



**Layer 1: components, signal routing and grounding**

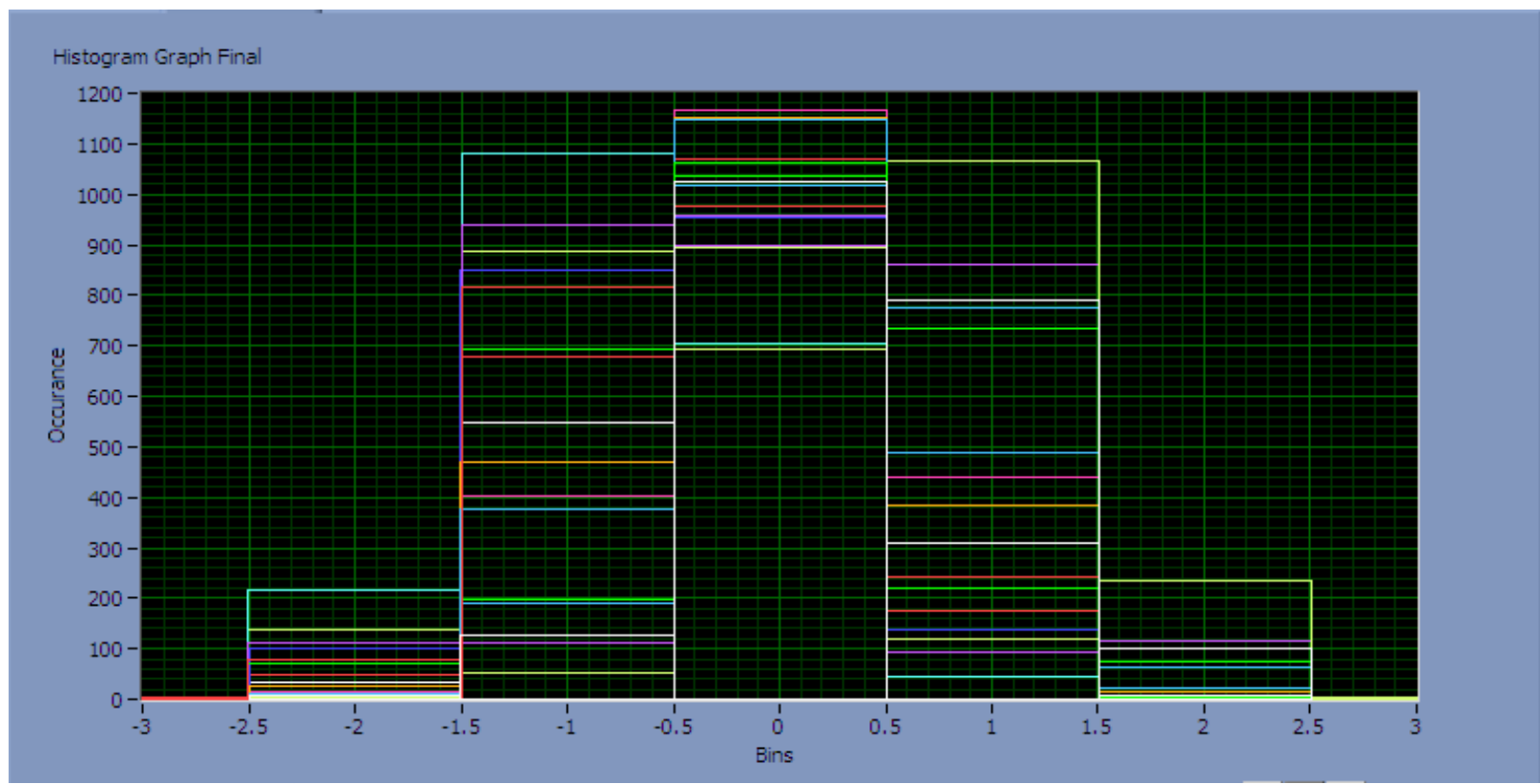
**Layer 2: ground plane**

**Layer 3: power/ground plane and ref routing**

**Layer 4: signal routing and soldering**

# 16 Channel Histogram

## Optimised Channel to Channel Matching



# Smart Grid Applications and Trends

## Transmission & Distribution:

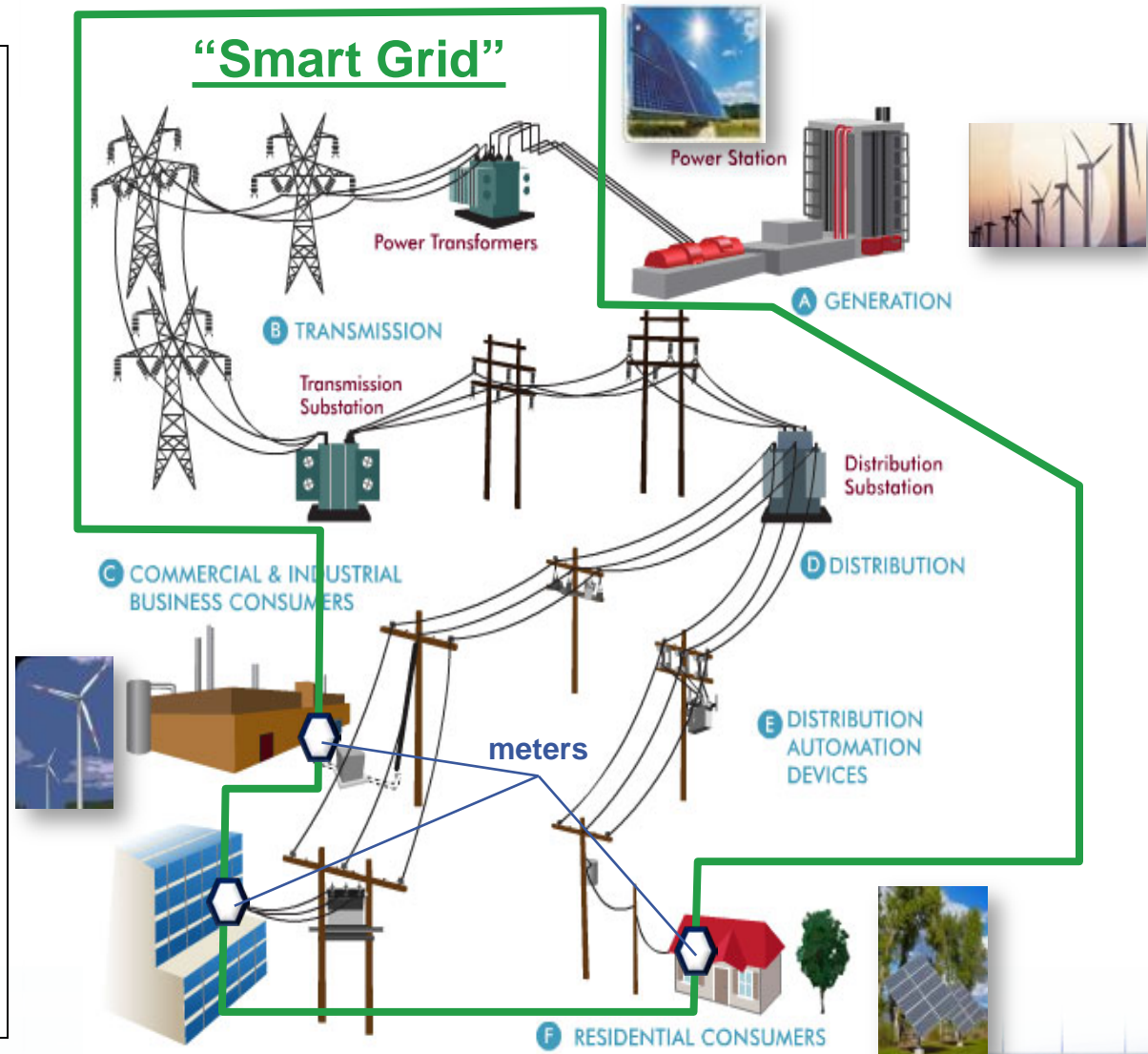
- Increasing grid measurement & control
- New vs. upgraded infrastructure
- Advanced sensing technologies

## Smart Meter:

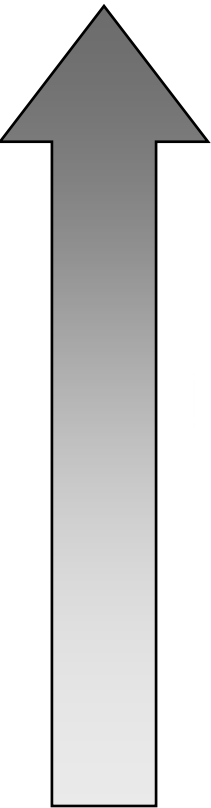
- Communications – RF or PLC
- Flexibility vs. cost
- High regional variation

## Solar/Wind Energy:

- Central inverters vs. micro inverters (solar)
- Government subsidy dependence
- Energy storage



# Power Line Monitoring Market - Voltage Segments



Category	Voltage level	Classification	Front-end Needs	Processor Needs
High End Voltages	> 110 kV	Power Bus Monitoring, Power generation stations	Simultaneous Sampling Dynamic Range	Fast response Minimal latency Floating point DSP Multiprocessing
Mid-End Voltages	<110 kV, >3.5kV	Power Bus Monitoring	Functionally the same as high-end, Reduced performance compared to high-end	Fast response Minimal latency Floating point & Fixed Point math Multiprocessing in some cases
Low End Voltages	<3.5 kV	Power Line Monitoring / Protection	Multiplexed 14/16 bit-ADC	Typically Fixed Point DSP Connectivity

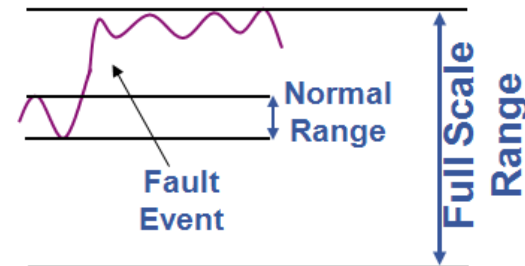
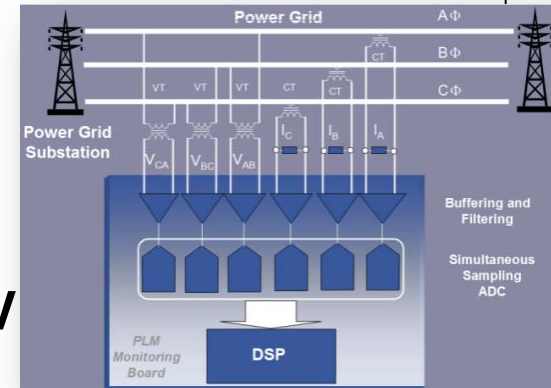


# Substation Automation

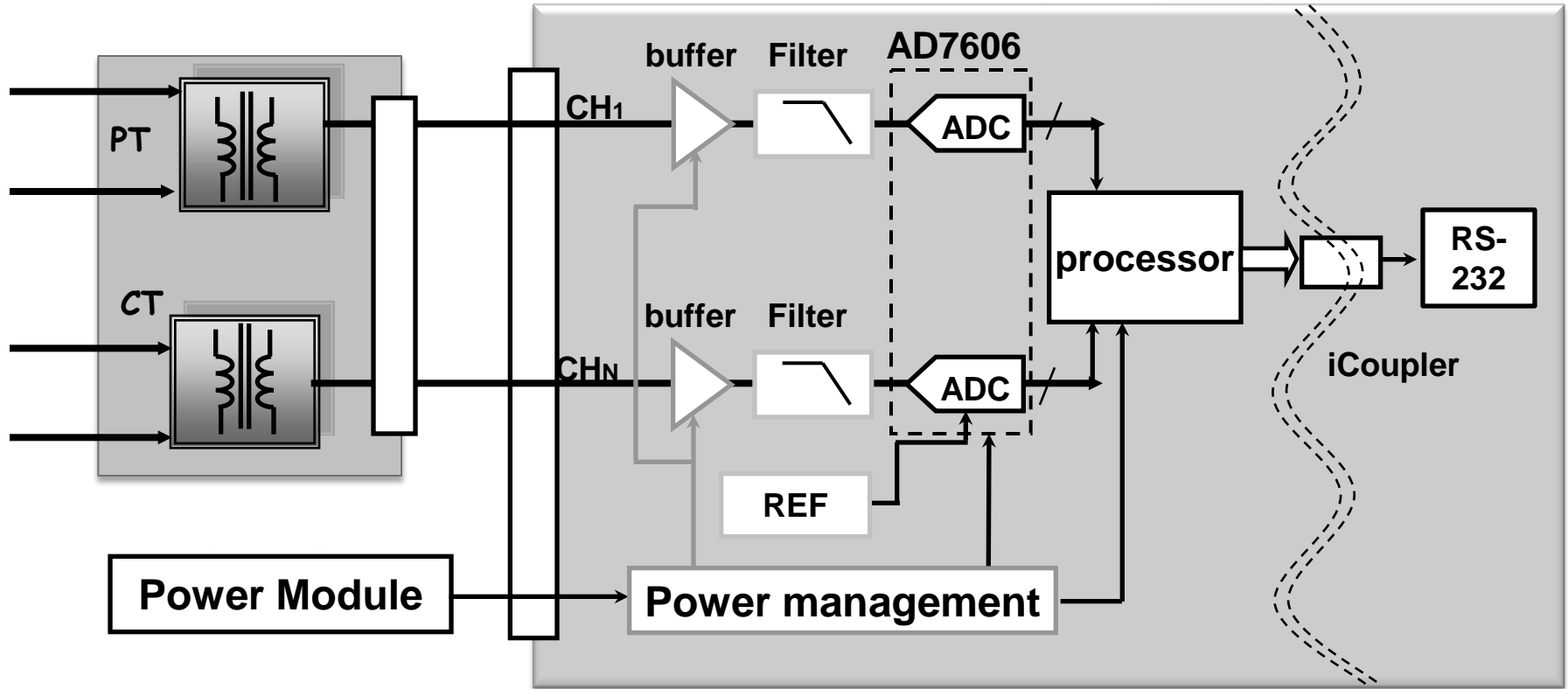
- ◆ Power grid – becoming more complex
  - Developing economies, upgrading, SMART grid
- ◆ Higher kV transmission
- ◆ Customers require increased monitoring and protection
  - Continuity of supply
  - Power Quality
  - Fault Detection e.g. Lightning strikes

## “Relay Protection & Measurement” - 35kV to 500 kV

- ◆ Preserve phase information – time stamp data
- ◆ Sample I & V to capture over/under I & V conditions.
- ◆ 16 bit resolution requirement to provide wide dynamic over/under Current and Voltage conditions
- ◆ Bipolar ADC capability

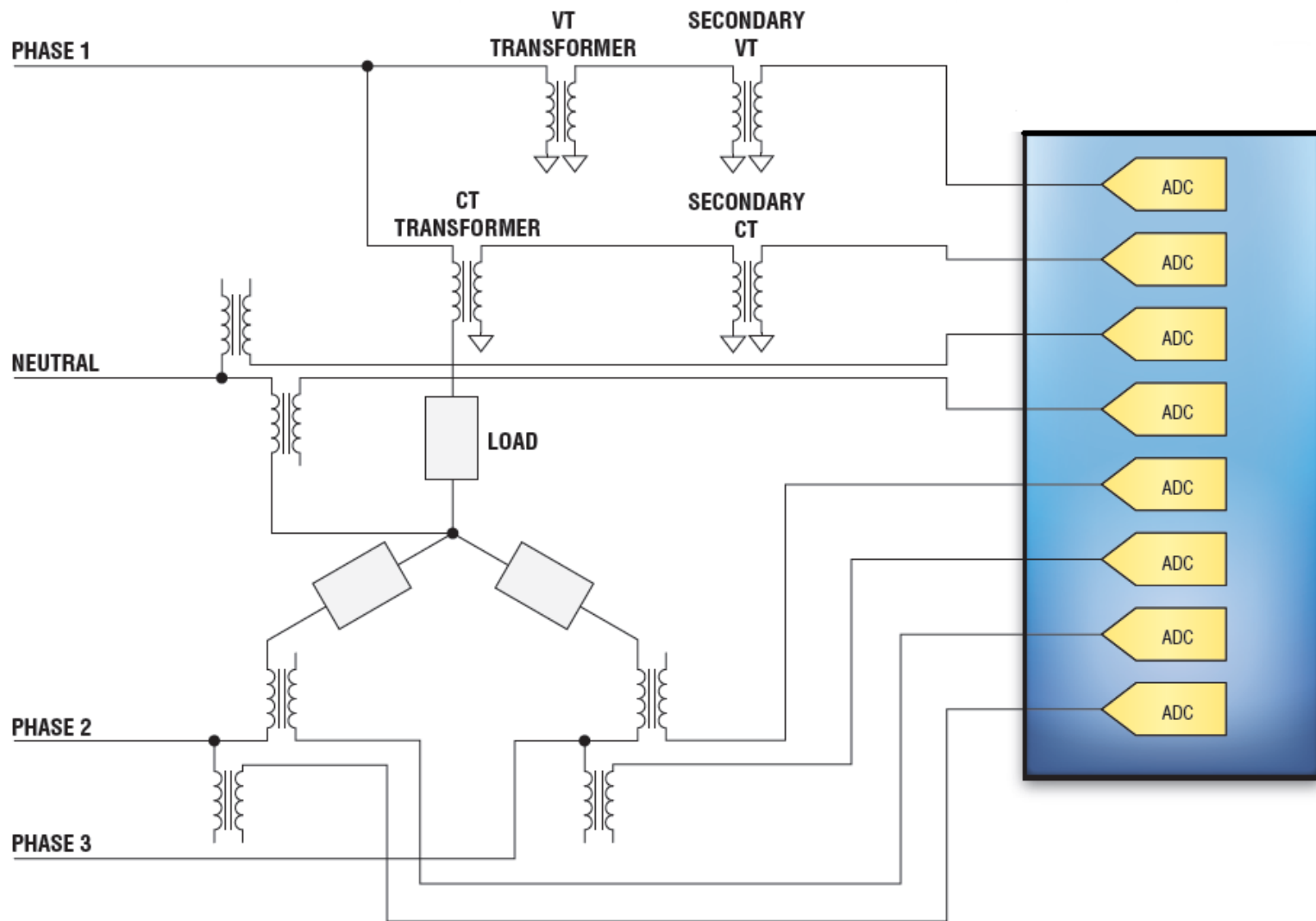


# Protection and measurement SA Application

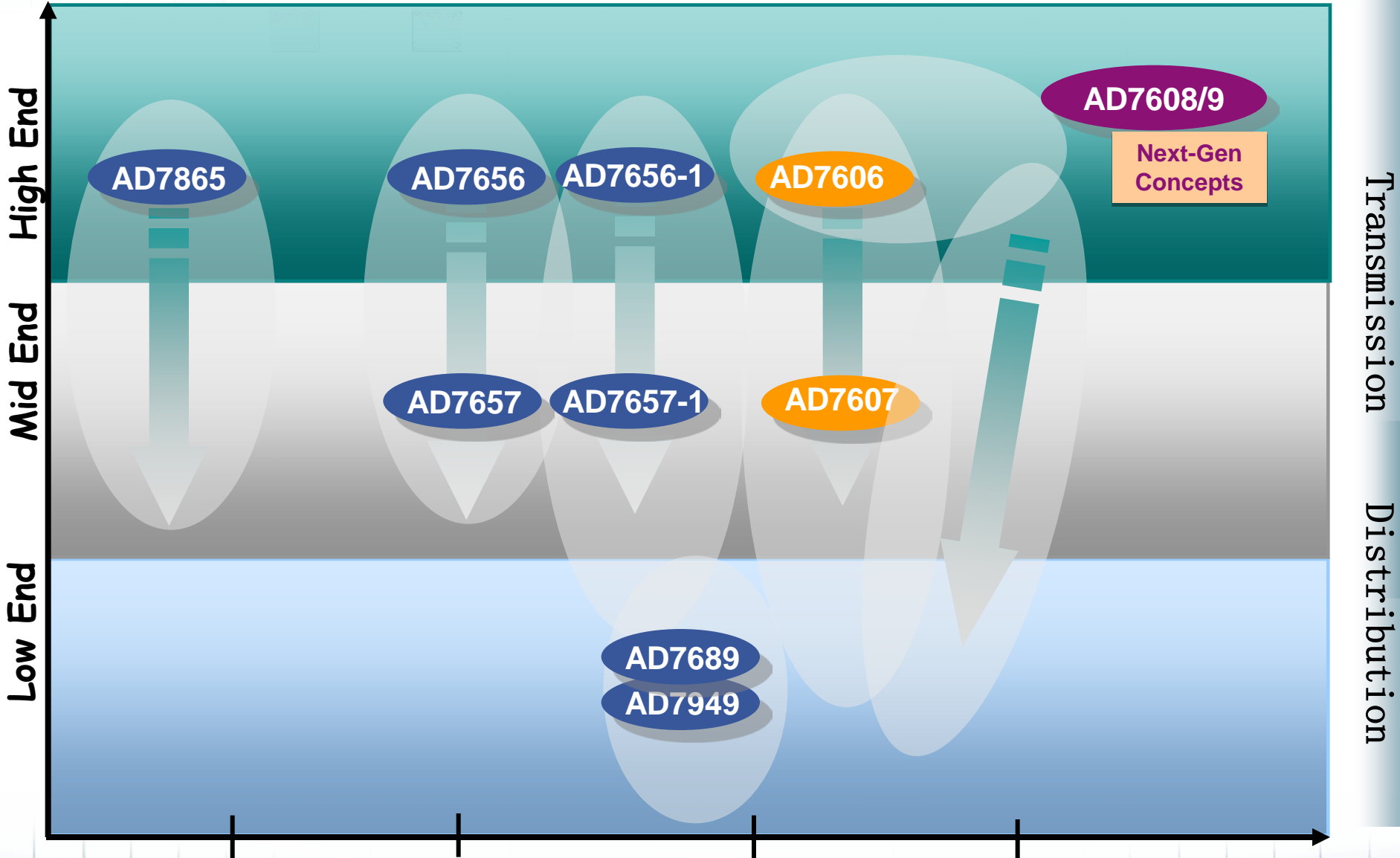


*Monitor 3 x I, 3 x V, and I & V in Neutral.*

# 8 channel sample with voltage and current monitoring of neutral line

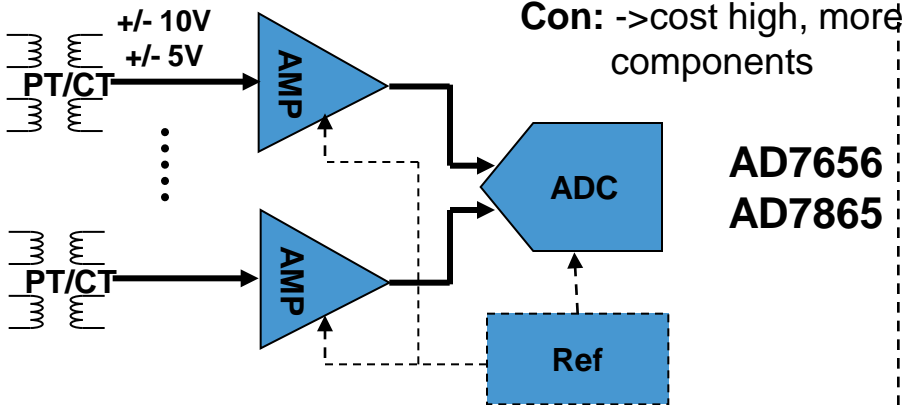


# ADI's ADC in power line application

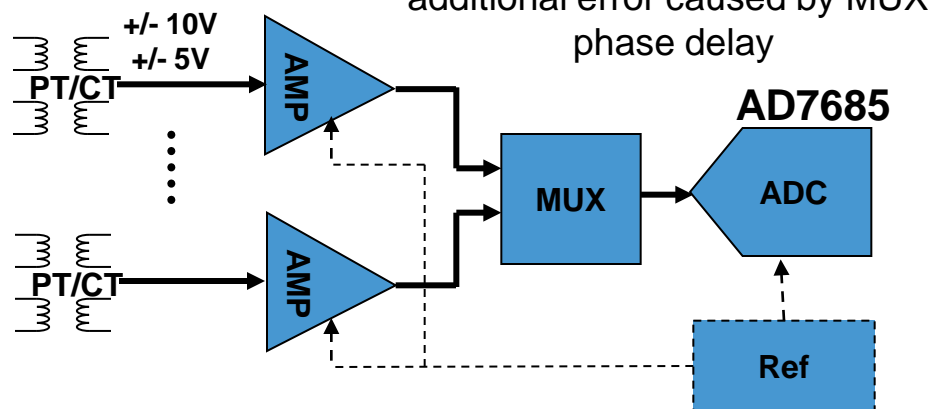


# Analog Front Ending Circuit

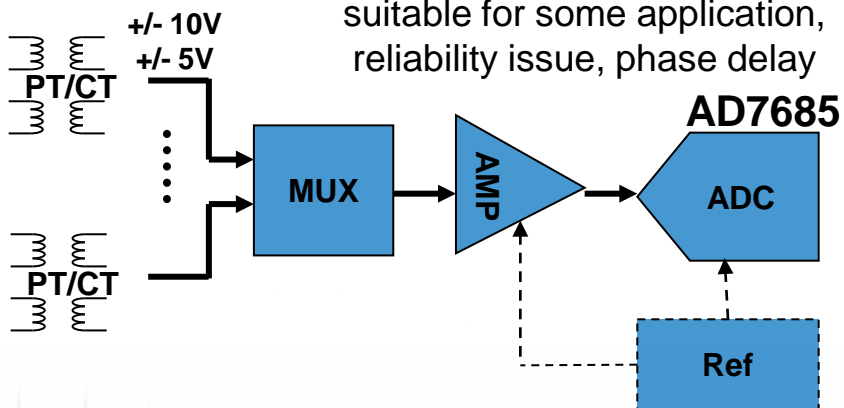
## Topology 1



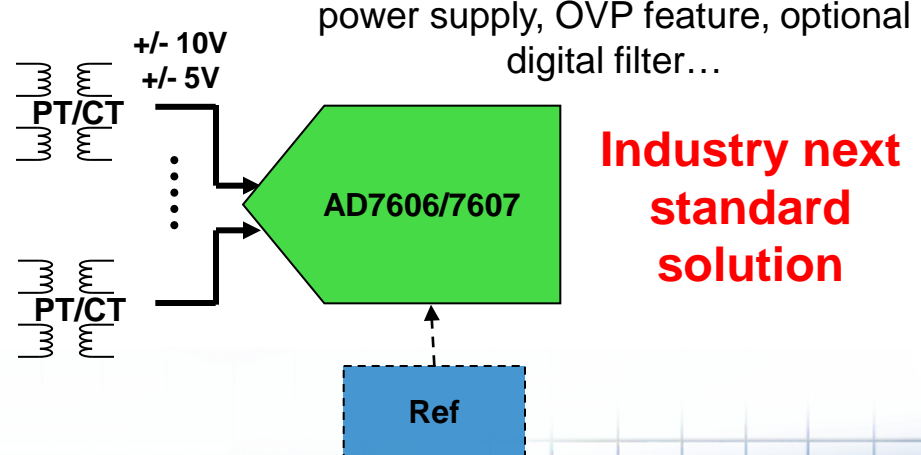
## Topology 2



## Topology 3



## Topology 4



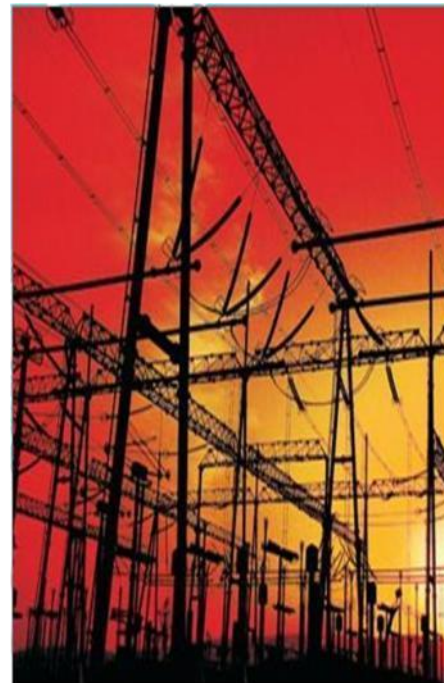
# Typical application in power line

## Fault protection

- ❑ Over current protection
- ❑ Under/Over voltage protection
- ❑ Frequency deviation detection and protection
- ❑ Unbalance/phase sequence error protection
- ❑ Earth-fault detection and protection
- ❑ ...

## Power quality monitoring

- ❑ Current/Voltage RMS value measurement
- ❑ Frequency measurement
- ❑ Harmonic content measurement
- ❑ Active/Reactive power measurement
- ❑ Power factor measurement
- ❑ Fault record
- ❑ Substation device status online diagnose
- ❑ ...



# Main Challenges & System Considerations

- ◆ **Robustness and reliability**
- ◆ **Wide signal dynamic range and high system accuracy**
- ◆ **Multi-channels measurement**
- ◆ **Variant system communication and synchronization interface**
- ◆ **Challenge from IEC61850**
- ◆ **Cost sensitive in some low/middle voltage application**

# Select the ADC for power line application

- High resolution ( $\geq 14$  bits ADC)

- High accuracy

- Good DC performance

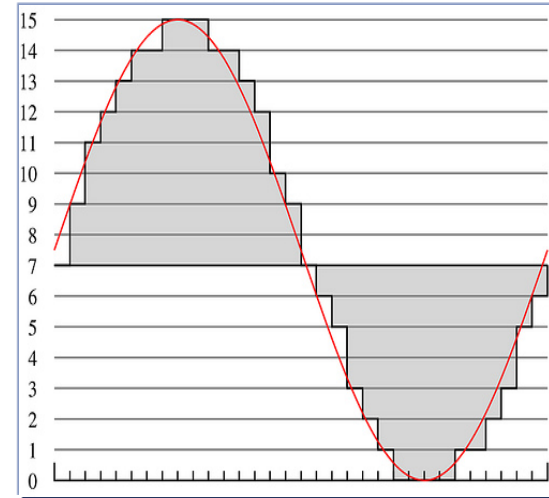
- INL, DNL typical value below 1 LSB

- Small gain and offset error

- Good AC performance

- Low distortion (THD  $< -80$ dB)

- High SNR and SINAD



- Multi-Channel with min. channel to channel difference and high channel to channel isolation

- High sample rate

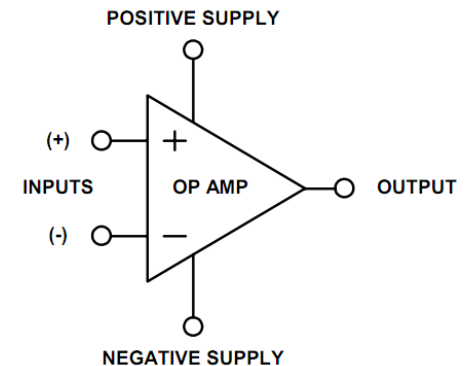
- High input signal range ( $\pm 10$ V;  $\pm 5$ V;  $\pm 2.5$ V)...

- High PSRR...



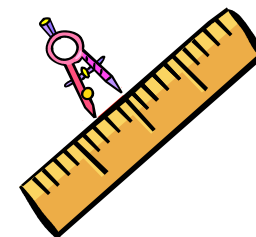
# Select OPAMP for power line application

- ❑ High open loop gain (>100db)
- ❑ Low Vos (<500uV) and low Vos temperature drift
- ❑ Low Input bias current ( $I_b < 2\text{nA}$ ,  $I_{os} < 1\text{nA}$ )
- ❑ Low noise (<20nV/ $\sqrt{\text{Hz}}$  and  $1/f$  Vp-p < 1uV)
- ❑ Big power supply span ( $\geq 24\text{V}$ )
- ❑ High CMR, PSR (>100db)
- ❑ Input voltage rang, no output phase reversal
- ❑ Unity gain stable

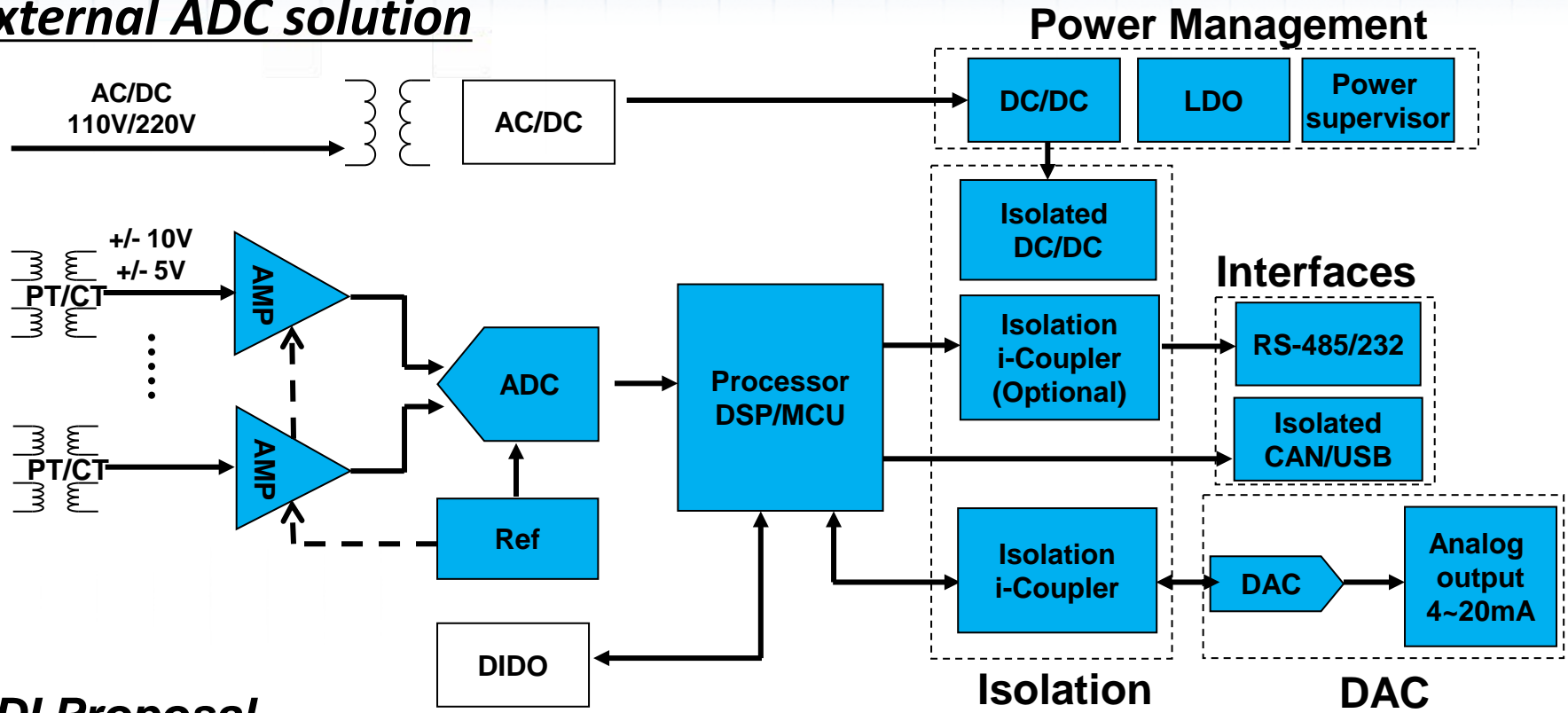


# Select the voltage reference for power line application

- ❑ High initial accuracy (0.1%)
- ❑ Good temperature coefficient (below 3ppm)
- ❑ Small time drift
- ❑ Low noise
- ❑ Drive capacity (5mA, 10mA...) for multi-components
- ❑ Load/Line sensitivity
- ❑ Low output impedance
- ❑ High PSRR



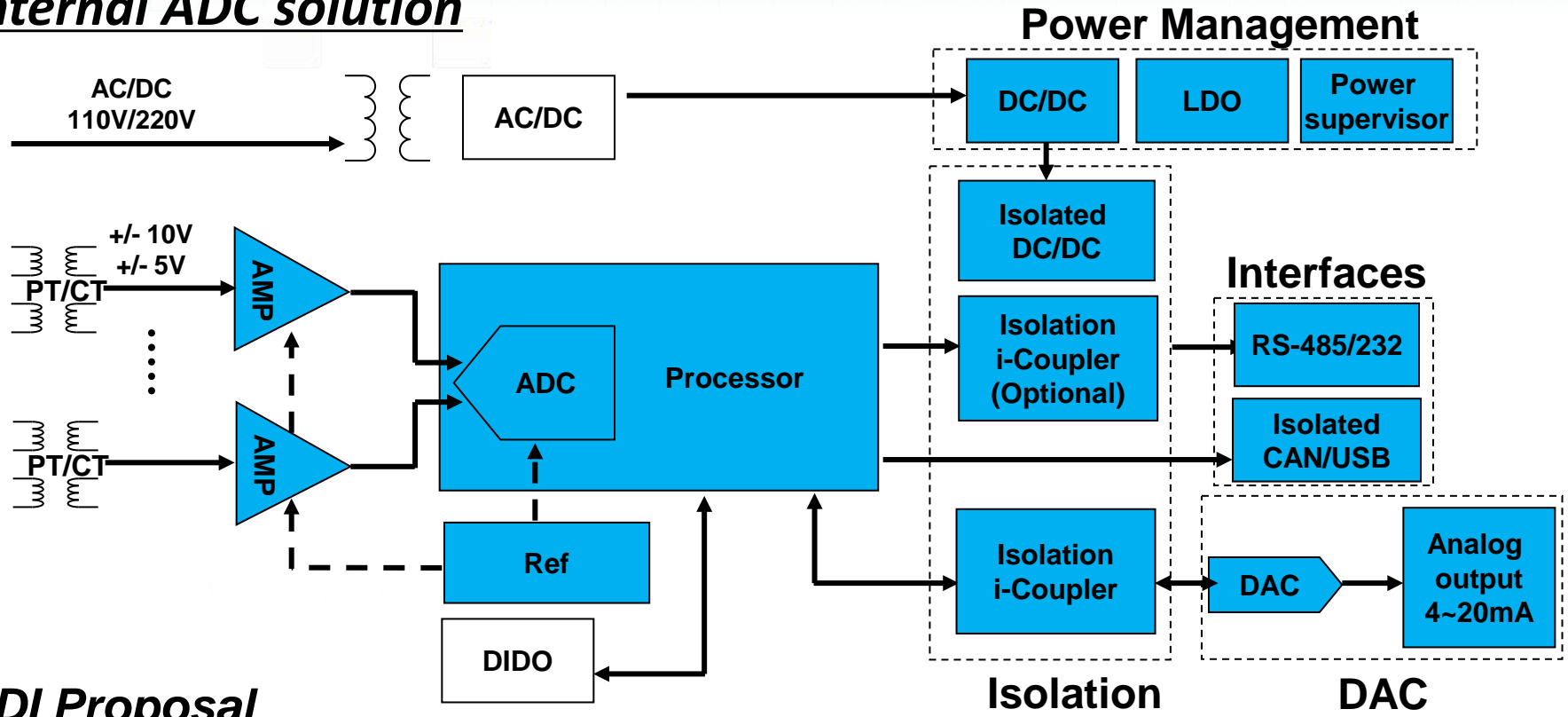
# External ADC solution



## ADI Proposal

Amplifier	ADC	Reference	Processor	Isolation	Interface	Power Management	DAC
<b>Bipolar</b> OP2177/4177 AD8672/8674, ADA4077-2, <b>Single Supply</b> AD8602/8604 AD8606/8608	<b>Simultaneous</b> AD7606/7607, AD7657-1/7658-1 <b>Non-Simultaneous</b> AD7327/7323 AD7689/7682 AD7490, AD7927 <b>Metering AFE</b> ADE7878	<b>Voltage reference</b> ADR42x ADR43x ADR34xx	<b>Fix point DSP</b> ADSP-BF512 ADSP-BF516 ADSP-BF518 <b>Float point DSP</b> ADSP-21489	<b>Power Isolation</b> ADuM5000 ADuM54xx  <b>Signal Isolation</b> ADuM141x	<b>RS485</b> ADM487E ADM2587E  <b>RS232</b> ADM3251E  <b>Isolated CAN</b> ADM3053	<b>LDO</b> ADP125  <b>DC/DC</b> ADP1612,ADP2301  <b>Multi-output (PMU)</b> ADP5034  <b>Power supervisor</b> ADM6710	<b>+/-10V &amp; 4~20mA output</b> AD5422

# Internal ADC solution



## ADI Proposal

Amplifier	Reference	Processor	Isolation	Interface	Power Management	DAC
<a href="#">Single Supply</a> AD8602/8604 AD8606/8608 AD8618 AD8666	<a href="#">Voltage reference</a> ADR34xx	<a href="#">Fix point DSP</a> ADSP-BF506F  <a href="#">ARM</a> ADuC702x	<a href="#">Power Isolation</a> ADuM5000 ADuM54xx  <a href="#">Signal Isolation</a> ADuM141x	<a href="#">RS485</a> ADM487E ADM2587E  <a href="#">RS232</a> ADM3251E  <a href="#">Isolated CAN</a> ADM3053	<a href="#">LDO</a> ADP125  <a href="#">DC/DC</a> ADP1612,ADP2301  <a href="#">Multi-output (PMU)</a> ADP5034  <a href="#">Power supervisor</a> ADM6710	<a href="#">+/-5/10V &amp; 4~20mA output</a> AD5422



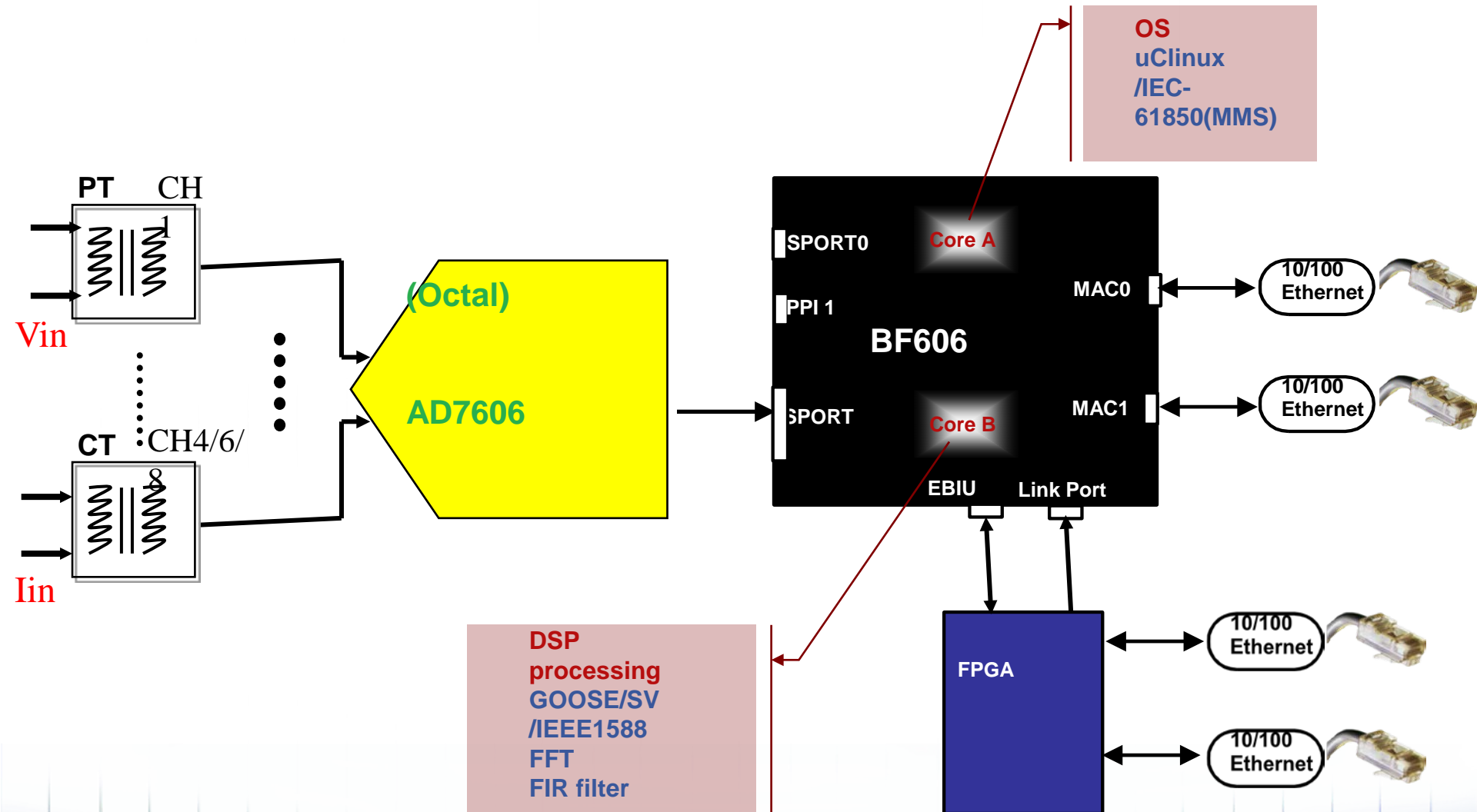
The World Leader in High Performance Signal Processing Solutions

# Power Line Monitoring (PLM) Reference Design

on BF606

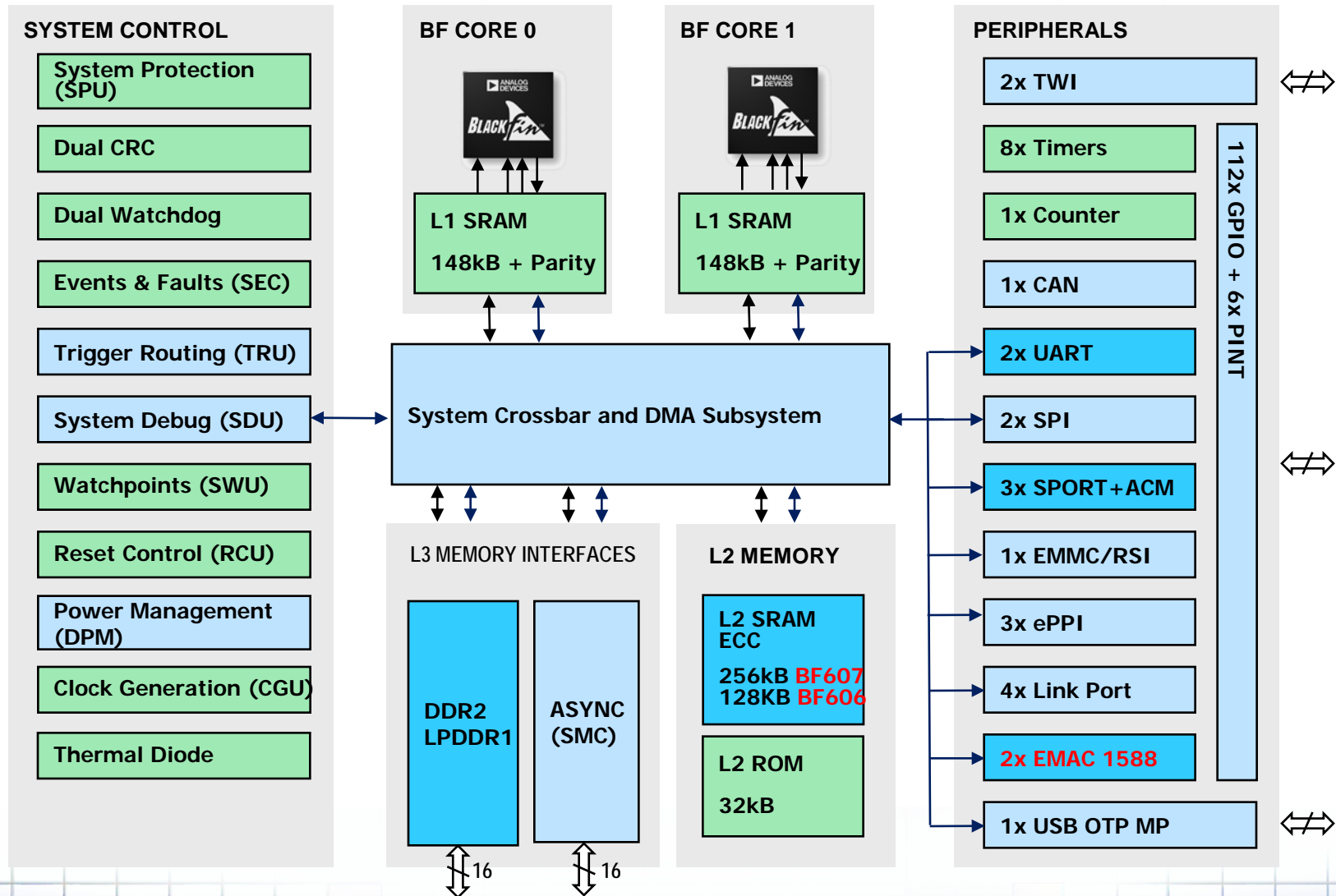


# PLM Reference Design (key signal chain)



# ADSP-BF607/6 Block Diagram

■ Part of Safety Concept

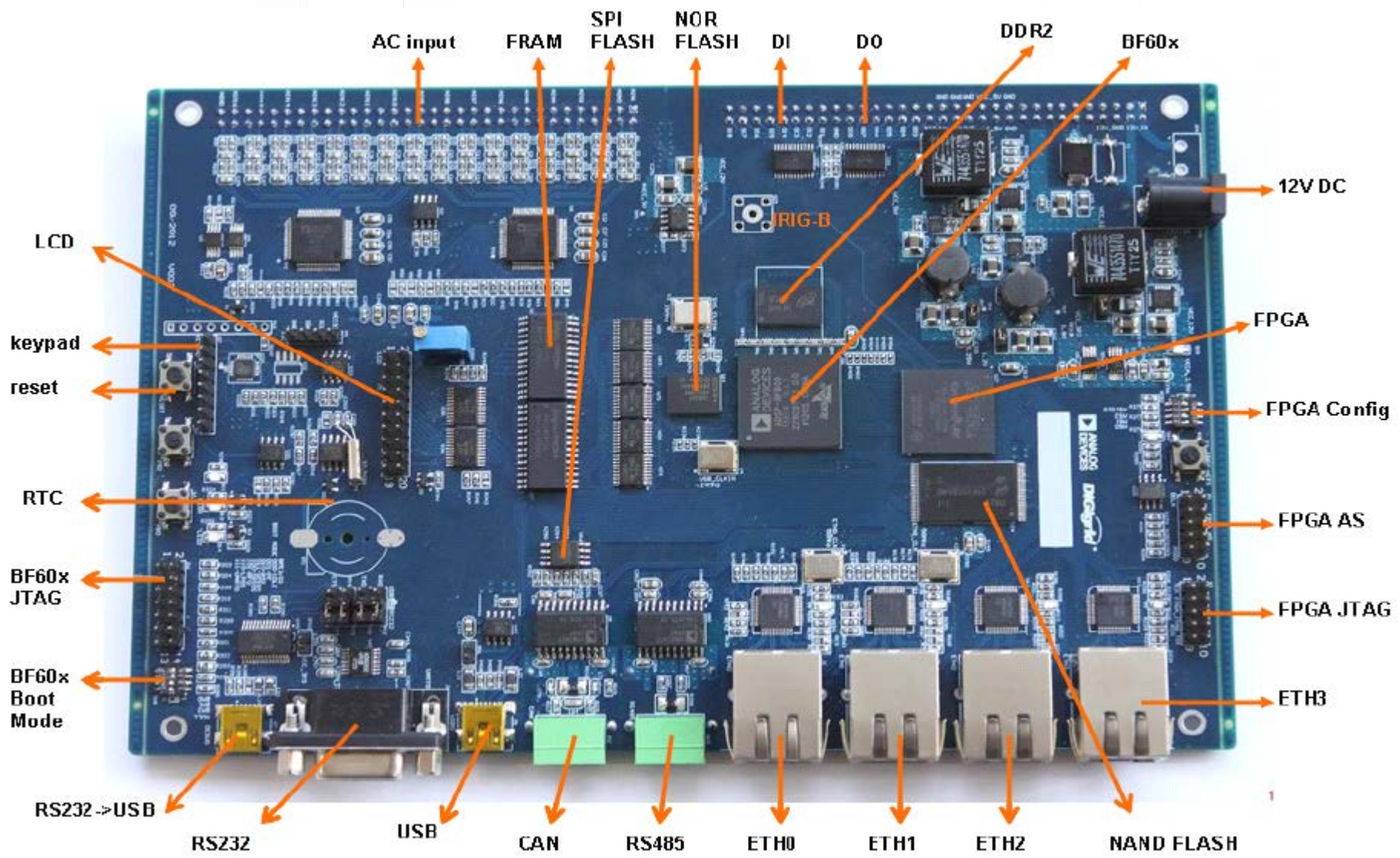


# A picture of PLM demo (BF606)

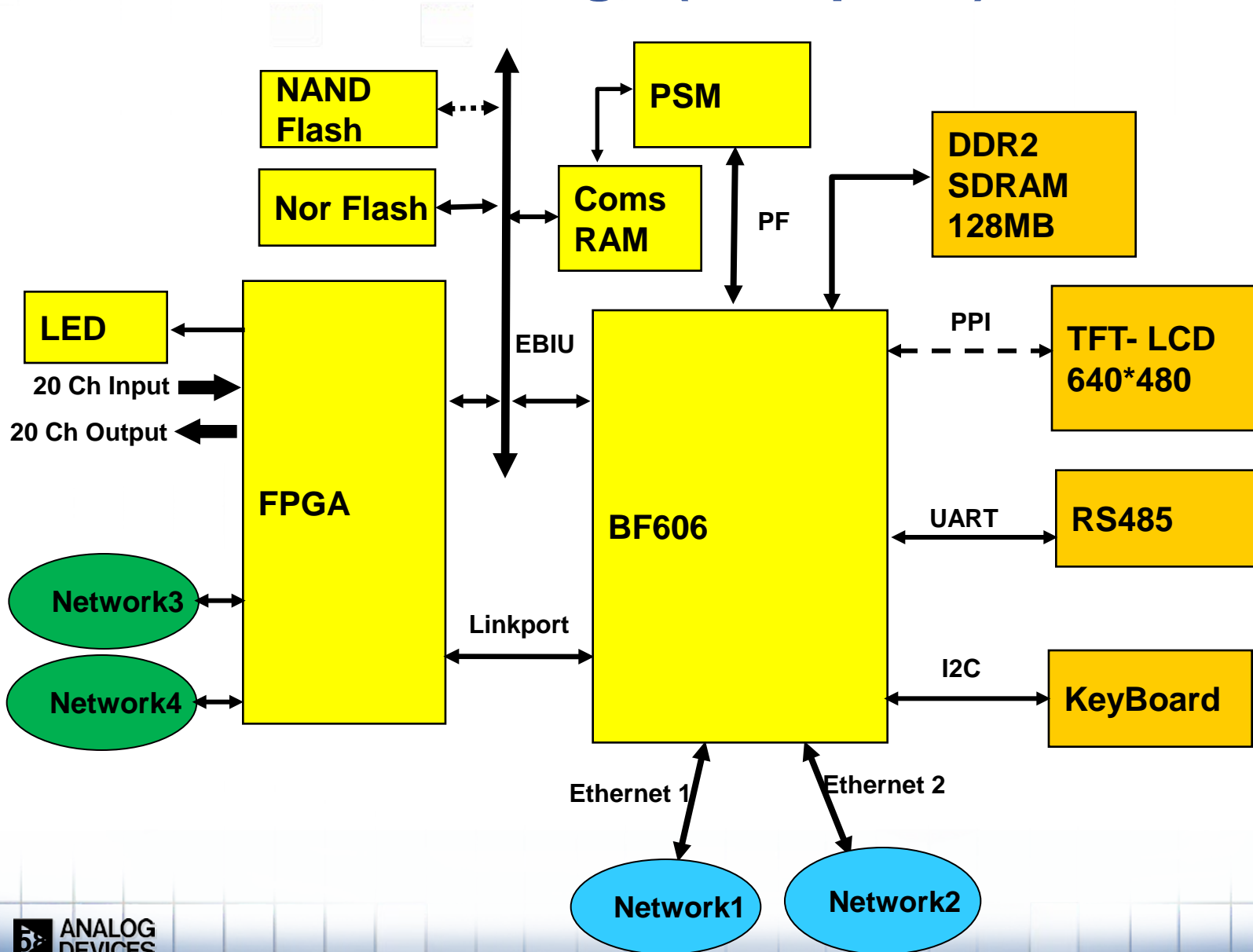




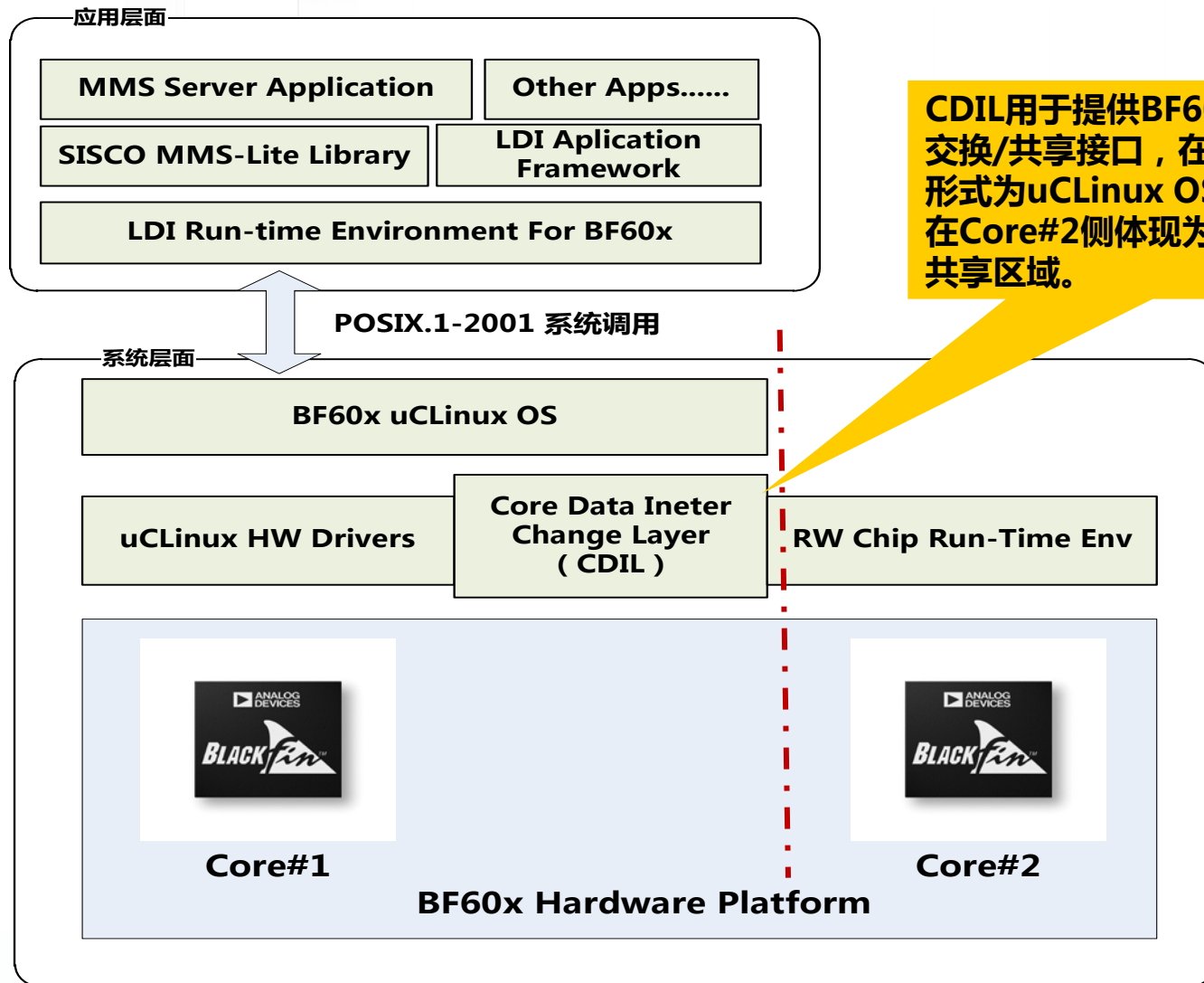
# Picture of DSP/ADC board



# PLM Reference Design (CPU parts)



# Software structure on BF606



CDIL用于提供BF60x双核间的数据交换/共享接口，在Core#1侧可能的形式为uCLinux OS下的内核驱动，在Core#2侧体现为一段寄存器/内存共享区域。

# Software code on BF606

- **硬件测试程序**

- 串行口通讯测试程序
- CAN口通讯测试程序
- 键盘操作及LCD液晶显示测试程序
- 网络口通讯测试程序
- LED控制测试程序
- 硬件WatchDog测试程序

- **应用软件**

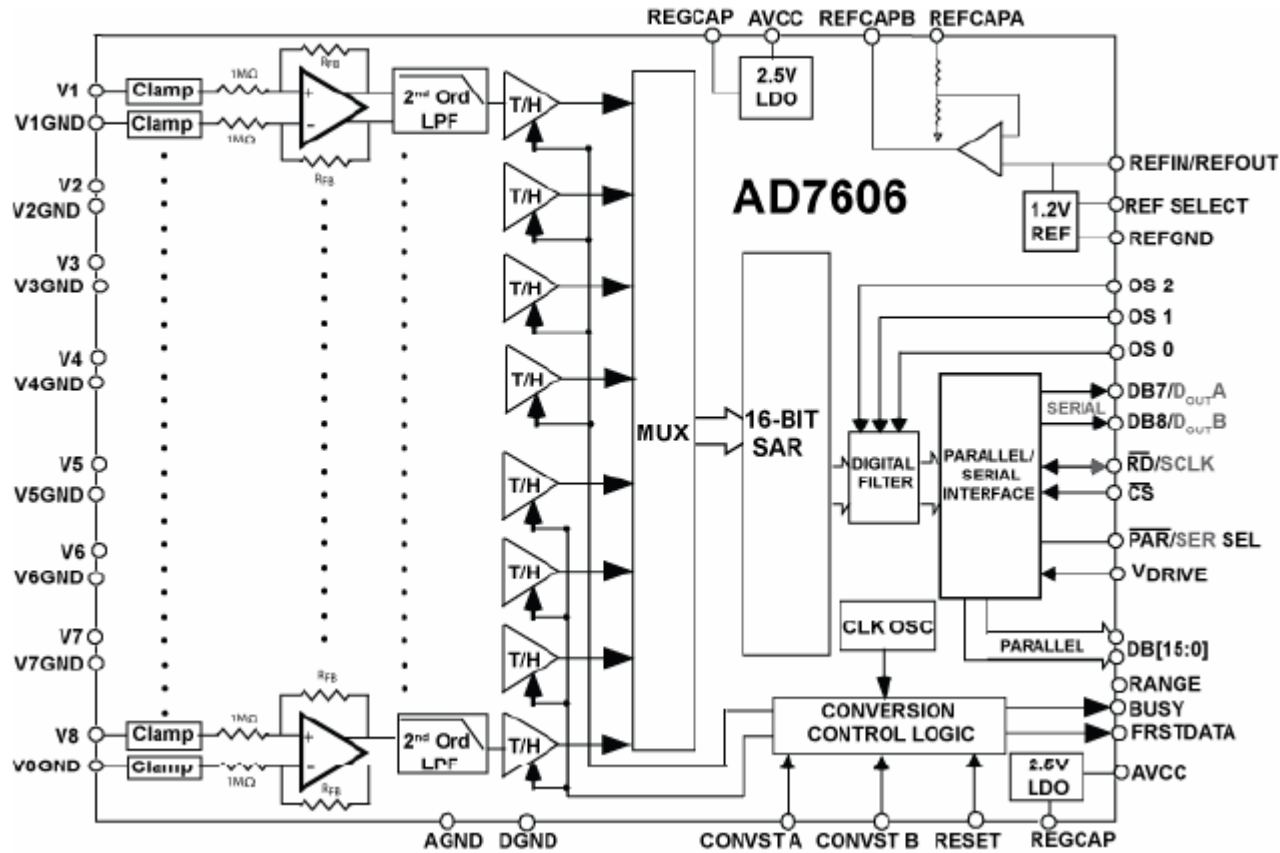
- 简单的保护设备HMI软件（保护定值配置、通讯参数配置及当前运行量显示浏览）
- IEC61850 MMS服务端实现
- GOOSE Publish实现
- 标准的Modbus Master/Slave实现
- 设备远程诊断维护服务（可选）

# BF60x Dual-Core Portfolio Summary (prelim)

Device	Market	MHz	L1 SRAM (kbytes)	L2 SRAM (kbytes)	Video Subsystem	Key Common Features	Package	Max Temp. (ambient)
<b>BF607</b>	Industrial & GP	500	148K/core	256K (ECC)	-	External Memory: 16-bit DDR2-500  3x ePPI (Camera/LCD/Parallel) USB2.0OTG HS multi-pt, CAN2.0, 2x Ethernet (w/1588), RSI/EMMC, 6x 1/2SPORT, 2x SPI, 2x UART, 2x PWM, 4x Link Port	19x19mm 0.8p CSP-BGA	85°C 70°C
<b>BF606</b>	Industrial & GP	400	148K/core	128K (ECC)	-			85°C 70°C

# AD7606 Functional Block Diagram

## FUNCTIONAL BLOCK DIAGRAM



# Key features on new PLM design

- ◆ **Dual-core processor (400/500MHz per core);**
  - The Blackfin core-A -- OS (uClinux);
  - The Blackfin core-B – GOOSE/SV/DSP processing;
- ◆ **Supporting 2 Ethernets port on-chip;**
  - Two independence MAC address;
- ◆ **Supporting IEC61850 protocol;**
- ◆ **One-Chip solution (OS and DSP in single BF606);**
- ◆ **Supporting up to 16-Chs Simultaneous Sampling ADCs (16-bit/16Chs ADC – AD7606);**
- ◆ **Supporting IEEE-1588v2 (optional);**
- ◆ **Supporting TFT-LCD (optional);**



# Software tools for PLM solution

- ◆ ADI 公司 CCES 1.0.1 开发环境;
- ◆ Ubuntu 10.04 环境 (Linux 编译环境);
- ◆ Buildroot 定制软件包
  - 交叉编译 bfin-toolchain
  - Uboot
  - uCLinux kernel 3.3.0 + ulmage/rootfs
- ◆ MMS Lite 软件包;



# MMS协议的验证 - IEDScout MMS

The image displays two windows from the IEDScout software. The left window, titled 'IEDScout', shows a 'Messages' log with the following text:

```
192.168.61.105: Initiate Response, status: SUCCESS
192.168.61.105: Requesting domain global names for Server
192.168.61.105: GetNameList response: domain global names for Server
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
LLN0.RP.urcbMeasure01.IntgPd
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
LLN0.RP.urcbMeasure09.FpItd
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
METMMKU1.CF.PF.phsC.units
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
METMMKU1.CF.W.phsB.units
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
METMMKU1.MX.A.phsB.instCVal.mag.f
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
METMMKU1.MX.PHV.phsA.cVal
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
P67P1PTOC1.DC.NamPlt.confIdRev
192.168.61.105: Requesting namedVariable names for Logical Device TEMPLATEBF
P6GGI01.CO.SPSCO05.Oper.orign.oIdent
192.168.61.105: GetNameList response: namedVariable names for Logical Device TE
```

The right window, titled 'Data View', shows a tree structure of data points with their values:

```
LN BKTxCBRT
LN DevIDLPHD1
LN LLN0
LN METMMKU1
FC MK
DO TotW {{ (0.000000e+00), (0.000000e+00), (0.000000000000) }}
DO TotVA1 {{ (0.000000e+00), (0.000000e+00), (0.000000000000) }}
DO TotVA {{ (0.000000e+00), (0.000000e+00), (0.01/01/1970_01) }}
DO TotPF {{ (0.000000e+00), (0.000000e+00), (0.01/01/1970_01) }}
DO Hz {{ (0.000000e+00), (0.000000e+00), (0.01/01/1970_01) }}
DO PPV {{ (0.000000e+00), (0.000000e+00), (0.000000e+00) }}
DO PHV {{ (0.000000e+00), (0.000000e+00), (0.000000e+00) }}
DA phsA
DA instCVal {{ (0.000000e+00), (0.000000e+00) }}
DA mag {{ (0.000000e+00), (0.000000e+00) }}
DA i 4.847000e+01
DA ang {{ (0.000000e+00), (0.000000e+00) }}
DA cVal {{ (0.000000e+00), (0.000000e+00) }}
DA q (0.000000000000)
DA t (u11/19/2012_05:45:34.000,0.000000000)
DA phsB
DA instCVal {{ (0.000000e+00), (0.000000e+00) }}
DA mag {{ (0.000000e+00), (0.000000e+00) }}
DA i 4.265000e+01
DA ang {{ (0.000000e+00), (0.000000e+00) }}
DA cVal {{ (0.000000e+00), (0.000000e+00) }}
DA q (0.000000000000)
DA t (u11/19/2012_05:45:34.000,0.000000000)
DA phsC
DA instCVal {{ (0.000000e+00), (0.000000e+00) }}
DA mag {{ (0.000000e+00), (0.000000e+00) }}
DA i 4.282000e+01
DA ang {{ (0.000000e+00), (0.000000e+00) }}
DA cVal {{ (0.000000e+00), (0.000000e+00) }}
DA q (0.000000000000)
DA t (u11/19/2012_05:45:34.000,0.000000000)
```

The status bar at the bottom of the Data View window indicates 'Report Overru' and '192.168.61.105: Completed'.

# Real-Time GOOSE 的测试方案



DO脉冲输出



```
Capture#0 @ 2010-09-25 15:44:55.857150  
Subscribe#0 Dest MAC: 01.0C.CD.01.00.01  
appid=0X4010, stNum= 2, sqNum= 12768  
confRev:1, test=0, allowedtoLive: 3000  
Event@ 2010-09-25 12:12:17.856208 q=0E  
Offset: -42us  
# 1 Time: 2010-09-25 12:12:17.856208 q=0E  
# 2 Bool[en]: 1  
# 3 Time: 2010-09-25 12:12:17.856208 q=0E  
# 4 Bool[en]: 0  
# 5 Time: 2010-09-25 12:12:17.856208 q=0E  
# 6 Bool[en]: 1  
# 7 Time: 2010-09-25 12:12:17.856208 q=0E  
# 8 Bool[en]: 0
```

捕获比对正确变化的GOOSE包，给出时间分析

# What can we provide in PLM Ref.design?

- ◆ **SCH of PLM Ref. design;**
- ◆ **PCB of PLM Ref. design;**
- ◆ **Drivers on BF60x;**
- ◆ **Stack on BF60x (TCP/IP, GUI, FAT32...);**
- ◆ **Materials in Chinese (中文资料) ;**



# ADI亚洲技术支持中心

- ◆ **ADI 客户支持中心热线电话: 4006-100-006 (24小时回复)**
- ◆ **模拟与其他线性产品技术支持: [china.support@analog.com](mailto:china.support@analog.com)**
- ◆ **嵌入式处理器DSP技术支持: [processor.china@analog.com](mailto:processor.china@analog.com)**
- ◆ **ADI中文网站: <http://www.analog.com/zh/index.html>**
- ◆ **ADI 亚洲技术支持中心网站:  
[http://www.analog.com/zh/content/ADI\\_CIC\\_index/fca.html](http://www.analog.com/zh/content/ADI_CIC_index/fca.html)**
- ◆ **ADI技术论坛: <http://bbs.ednchina.com/ADI/>**
- ◆ **ADI 技术论坛(英语) : <http://ez.analog.com/index.jspa>**



The World Leader in High Performance Signal Processing Solutions

# Thanks!

ADI中国地区技术支持热线：4006 100 006

ADI中国地区技术支持信箱：[china.support@analog.com](mailto:china.support@analog.com)

